VersaClock® 7 (VC7) Fanout Buffer Mode for PCI Express

This document describes the steps needed for the Renesas IC Toolbox (RICBox) to enable VC7 to initially output 100MHz using the onboard crystal as the reference, then switch to a CLKIN reference when a GPI/GPIO is toggled (PERST#). Fanout mode is only available for Bank4, Bank5, and Bank6. The RCx1012A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11. The RCx1008A fanout mode is supported on OUT8, OUT10, and OUT11. For more information about RICBox, see the Renesas IC Toolbox User Guide.

Contents

1. Bench Setup

Equipment used for this measurement are the RC21008A/RC31008A Evaluation Kit (EVK), Signal Generator, and Frequency Counter. The RC21012A/RC31012A EVK may be used as well.

1.1 Evaluation Board (EVB) Setup

Rework the evaluation board (EVB) so that CLKIN0 and/or CLKIN1 are connected to VC7. Refer to the RC21008A/RC31008A or RC21012A/RC31012A EVB schematics for more information. For this example, the clock inputs are DC coupled. The clock source will be connected to CLKIN0. GPIO0 and GPIO1 will be used for indicating Loss of Signal (LOS) and PERST#, respectively. Note that PERST1# is also available. Lastly, OUT10 will be connected to the frequency counter. OUT10 is used in this example because the crystal can be muxed out. It is highly recommended that the crystal frequency is trimmed by using external caps on the XIN/XOUT pins or by adjusting TOP.XO.XO_CNFG register fields en_cap_x1 and en_cap_x2.

1.2 Signal Generator Setup

Any of the accepted clock input types for VC7 can be used to setup the signal generator. Depending on the clock input type, adjust termination on the board or internally using RICBox.

1.3 Frequency Counter Setup

Setup the counter to accept 100MHz. If the VC7 EVB has AC-coupled outputs, adjust the counter to enable 50Ω termination.

1.4 RICBox Installation

For more information on installing RICBox software for VC7, see the Renesas IC Toolbox User Guide.

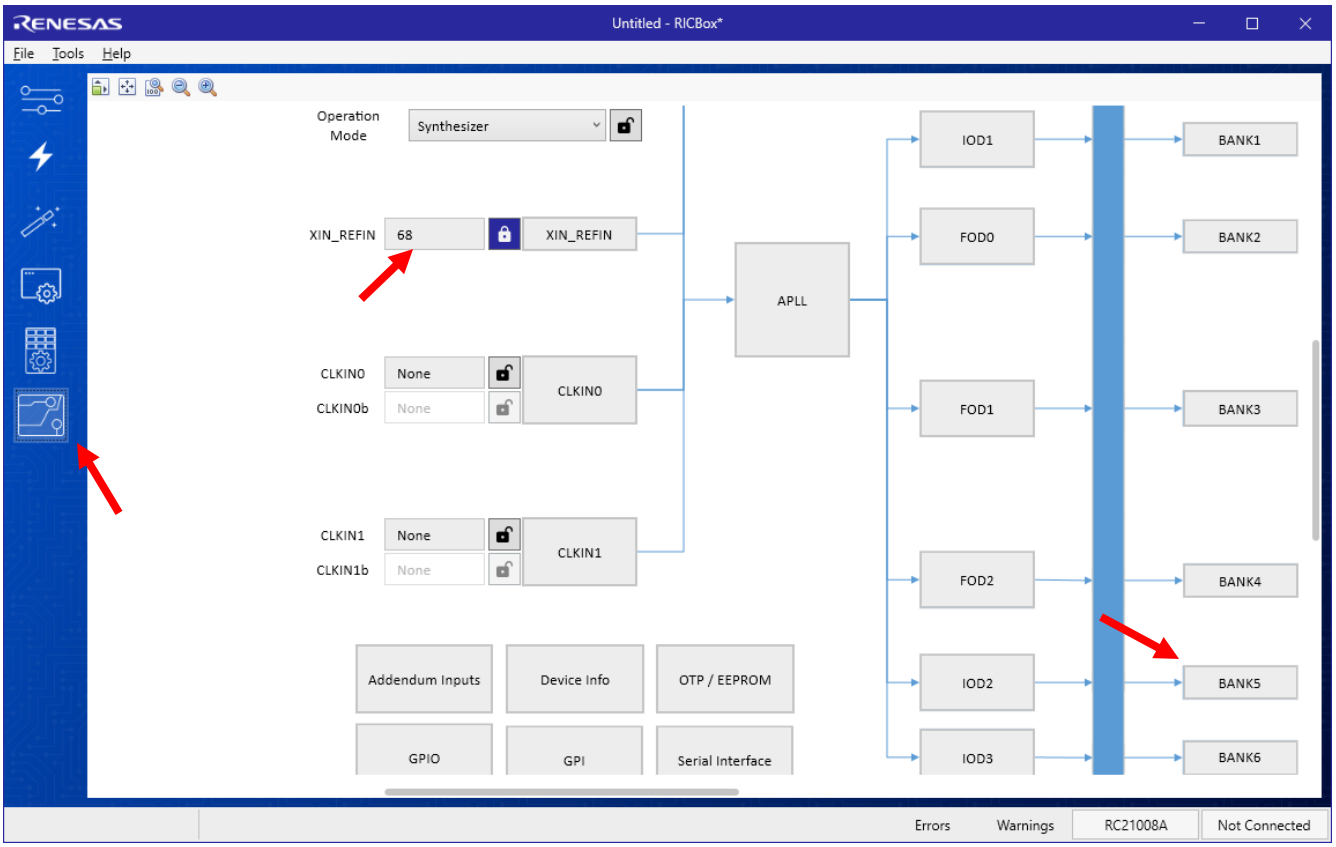
1.5 VC7 Setup

Use RICBox to trim the on-board crystal (optional), setup clock input, fanout buffer mode, clock output, and GPIO (LOS/PERST#).

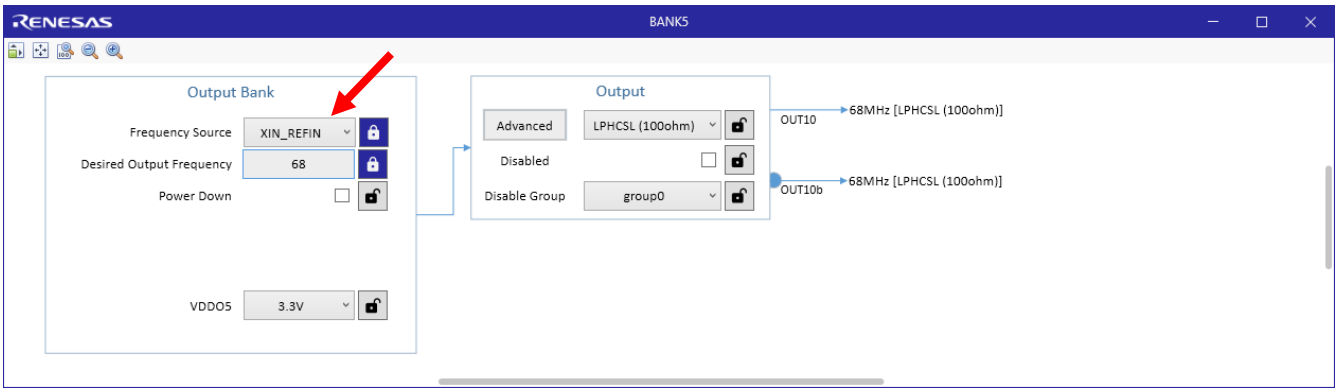
1.5.1 Trimming the Crystal (optional)

As previously mentioned, OUT10 will be the output to measure as the crystal signal can be muxed out. This step is optional but highly recommended. Otherwise, large PPM offsets will result in many little spurs in the phase noise plot.

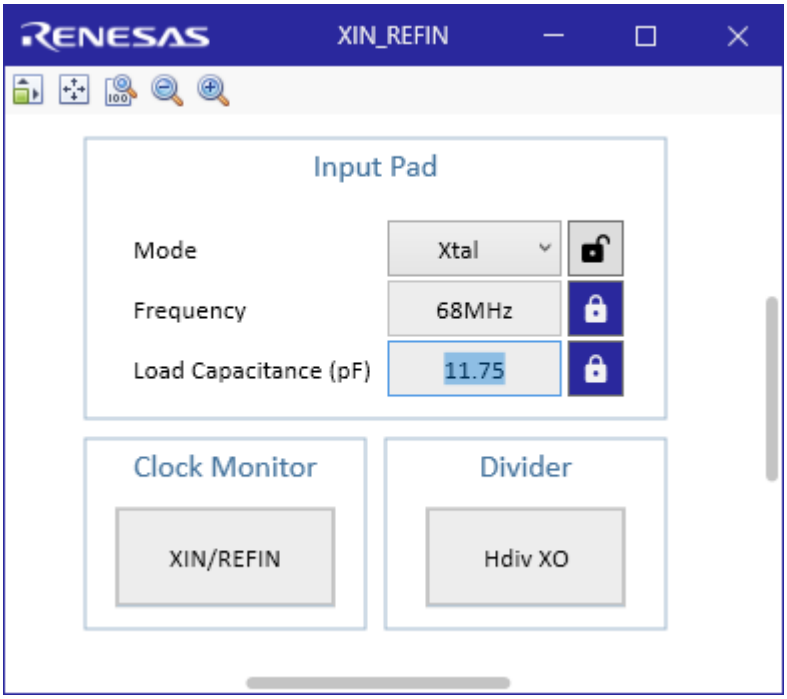
1. Start RICBox and create a new project.
2. Choose the product variant that matches the unit on the EVB.
3. During the wizard phase, simply click Finish.
4. View the block diagram. If your crystal is different from the default value, then update the XIN_REFIN frequency.



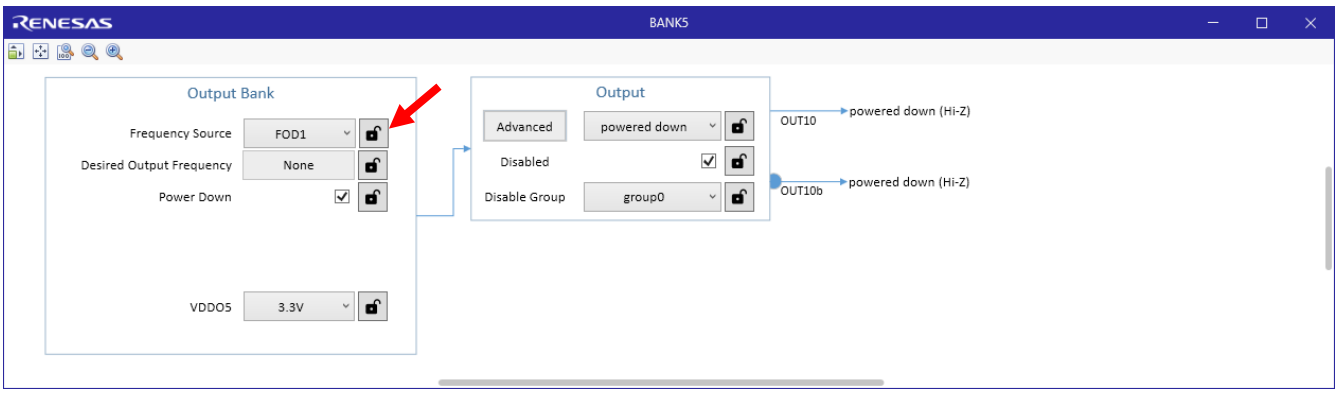
5. Click on Bank5 to bring up the sub-diagram window. For the *Frequency Source*, choose XIN_REFIN. Set the *Desired Output Frequency* to match the crystal frequency.



6. Connect and program VC7. Use the frequency counter to measure the crystal frequency. Go back to the main block diagram and click on the XIN_REFIN block to bring up the sub-diagram window. Adjust the *Load Capacitance* until the measure frequency by the counter is closest to your expected crystal frequency. Use 0.1 (pF) steps for the best results. After changing the load capacitance value, program VC7 again.



7. Close the XIN_REFIN sub-diagram window and go back to the Bank5 sub-diagram window. Click on the Blue Locks to reset the fields back to the GUI defaults.

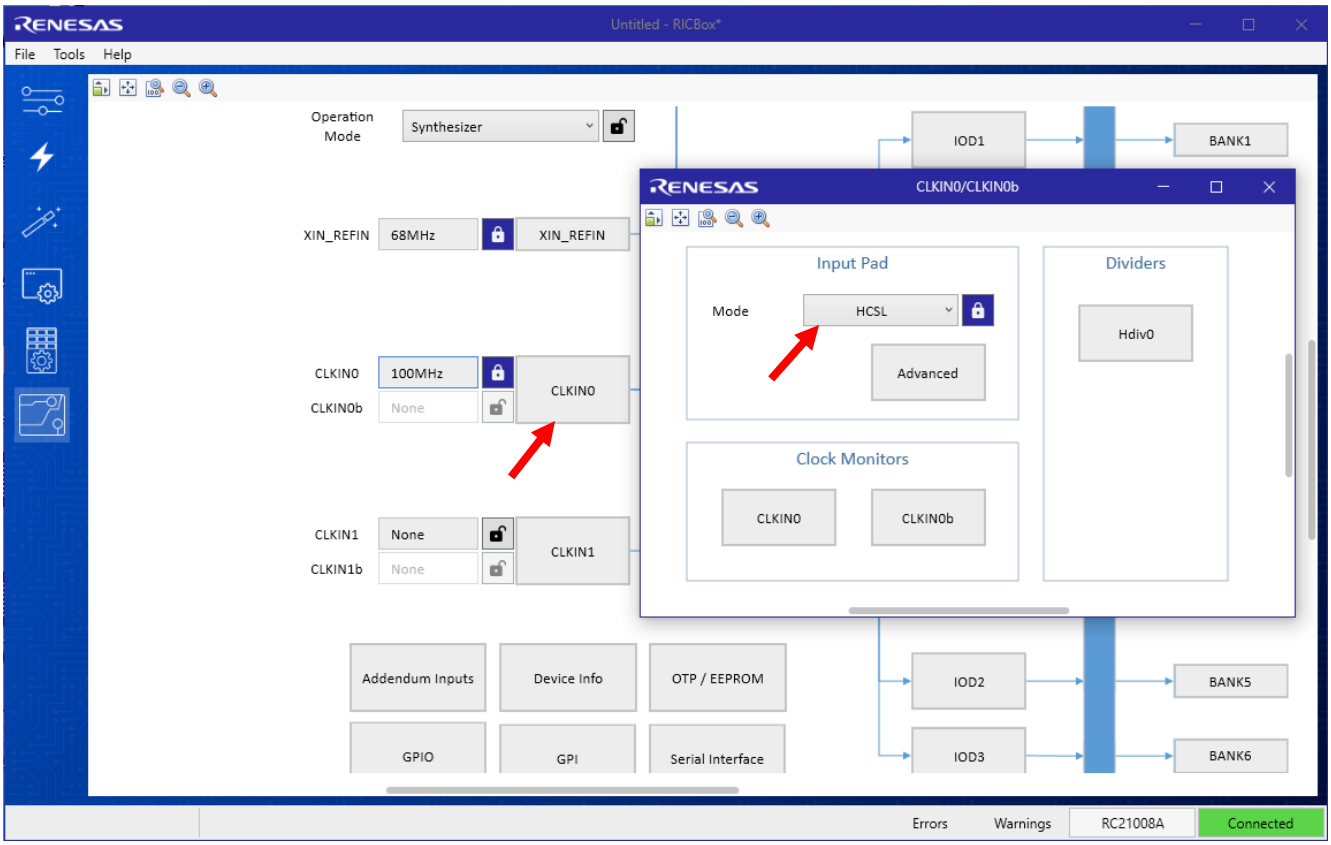


The onboard crystal is now trimmed.

1.5.2 Setting Up CLKIN

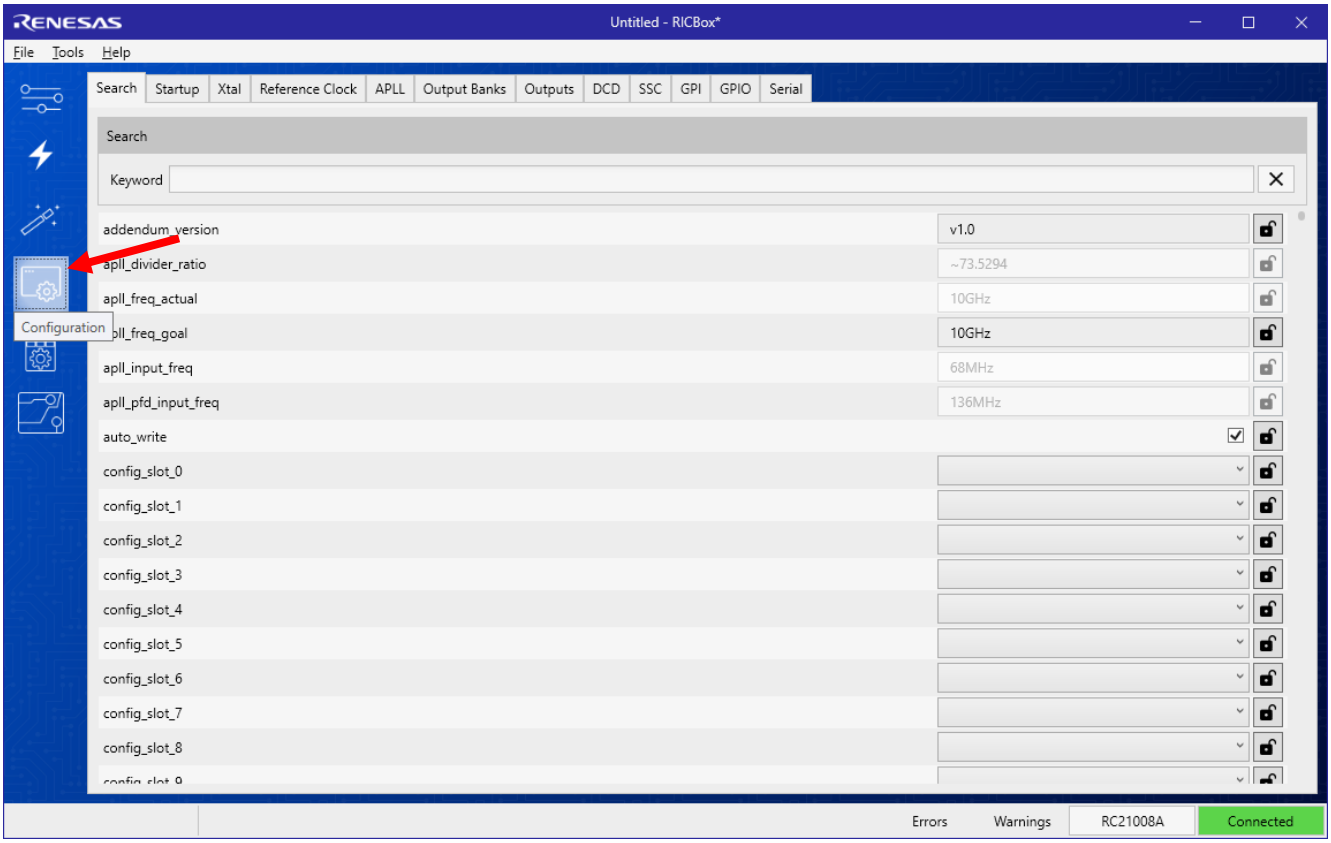
CLKIN0 or CLKIN1 – or both – may be used for the fanout source. For this example, CLKIN0 will be used. The following steps can also be applied to CLKIN1:

1. Start by setting the CLKIN0 frequency to 100MHz.
2. Push the CLKIN0 button to open up the sub diagram window.
3. Choose the appropriate mode to match your clock input type.
4. Close the CLKIN0 sub-diagram window when completed.

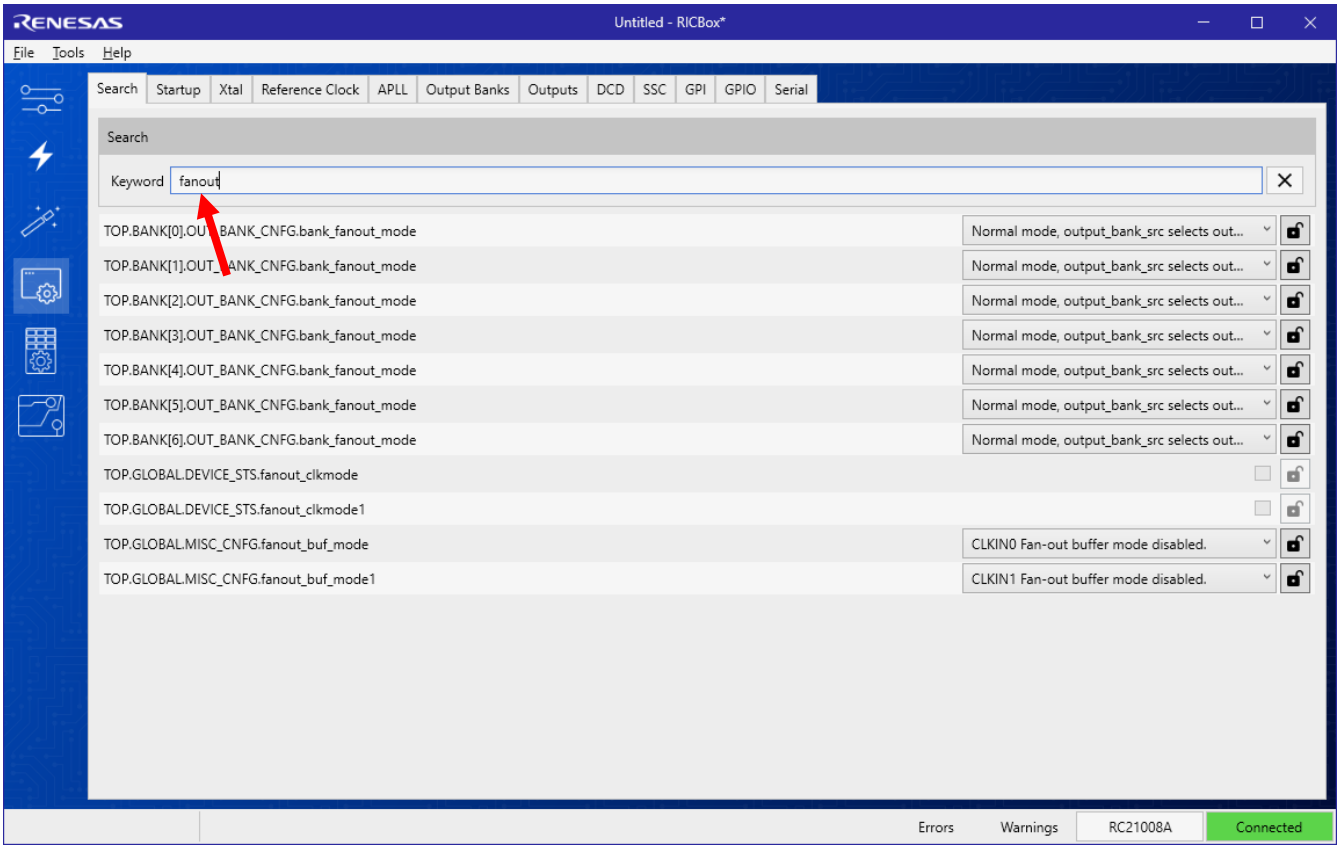


1.5.3 Fanout Buffer Mode

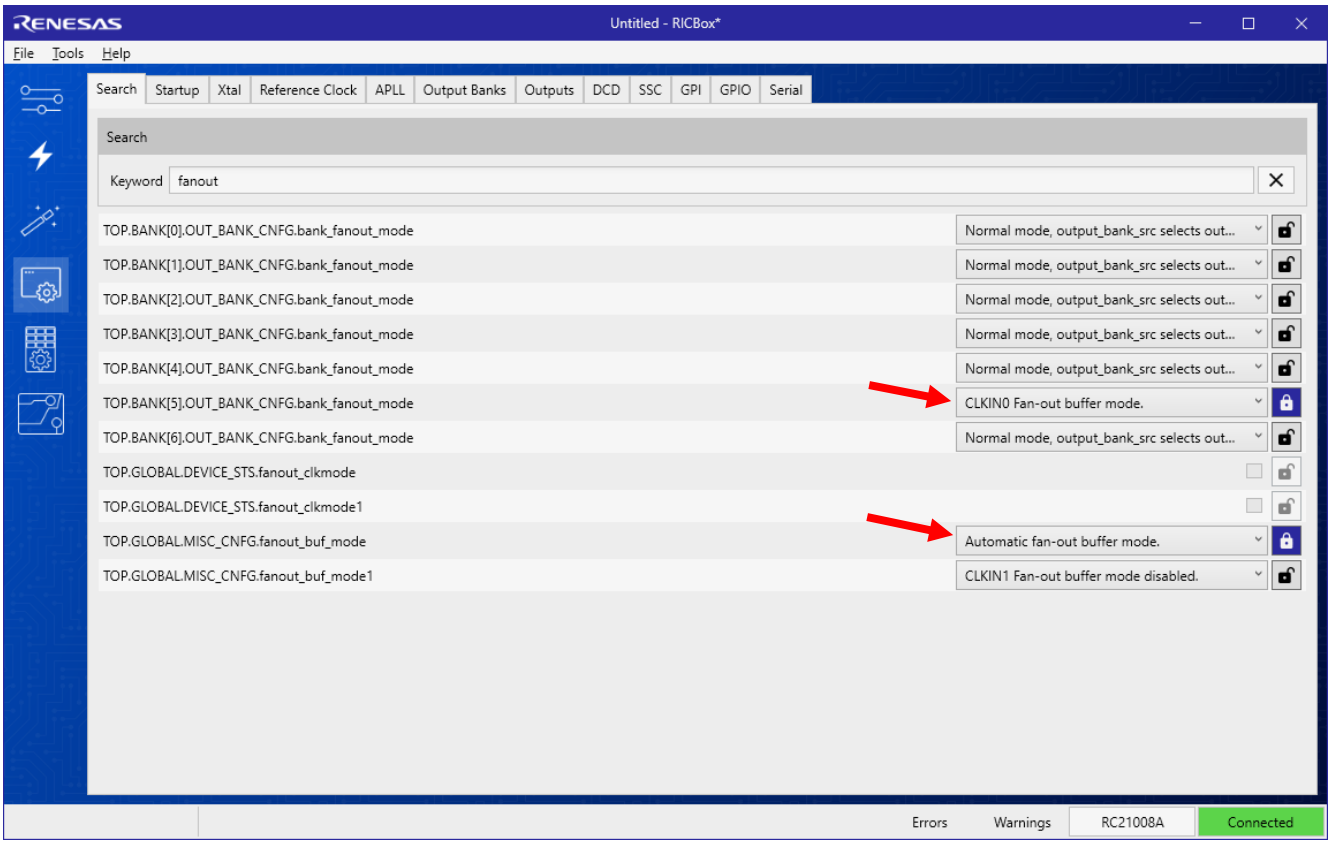
1. On the left of the RICBox window, click on the *Configuration* icon to view all the fields and register bit-sets.



2. In the search field near the top, type in “fanout” and push enter.



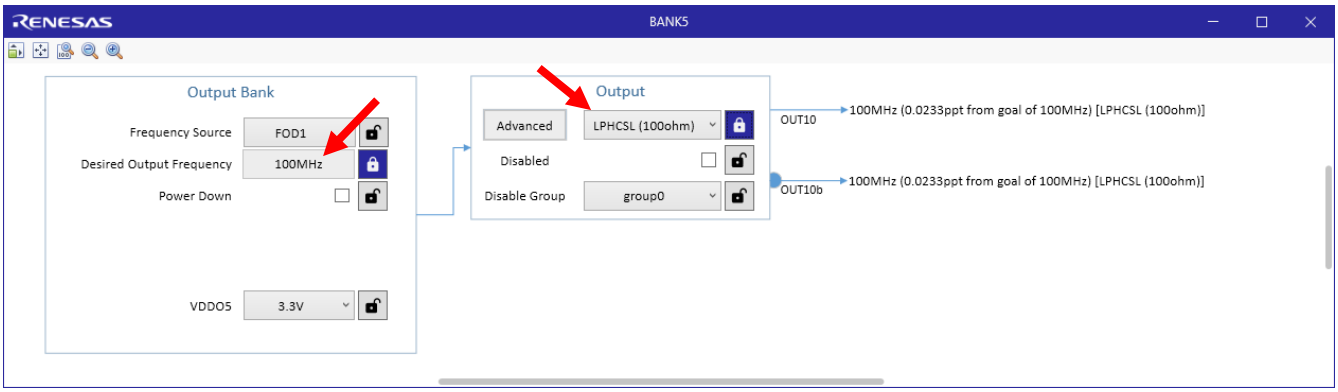
3. Bank4, Bank5, and Bank6 support fan-out buffer mode. OUT10 (Bank5) will be used for this example. As a result, the register field **TOP.BANK[5].OUT_BANK_CNFG.bank_fanout_mode** will need to be updated to select CLKIN0 fanout buffer mode.
4. Next, update **TOP.GLOBAL.MISC_CNFG.fanout_buf_mode** to *Automatic fan-out buffer mode*.



1.5.4 Setting Up OUT10

Click on the block diagram icon on the left side of RICBox window to display the main block diagram again. Click on Bank5 button to bring up the sub-diagram window.

1. Enter the desired output frequency (100MHz).
2. Choose the appropriate output type.
3. Close the sub-diagram window when completed.

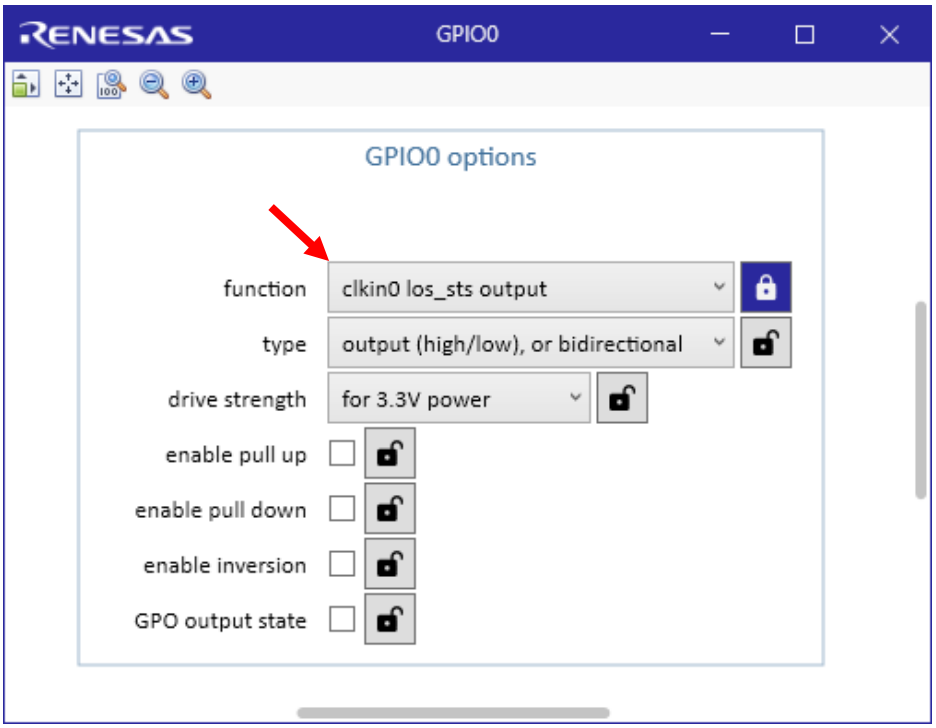


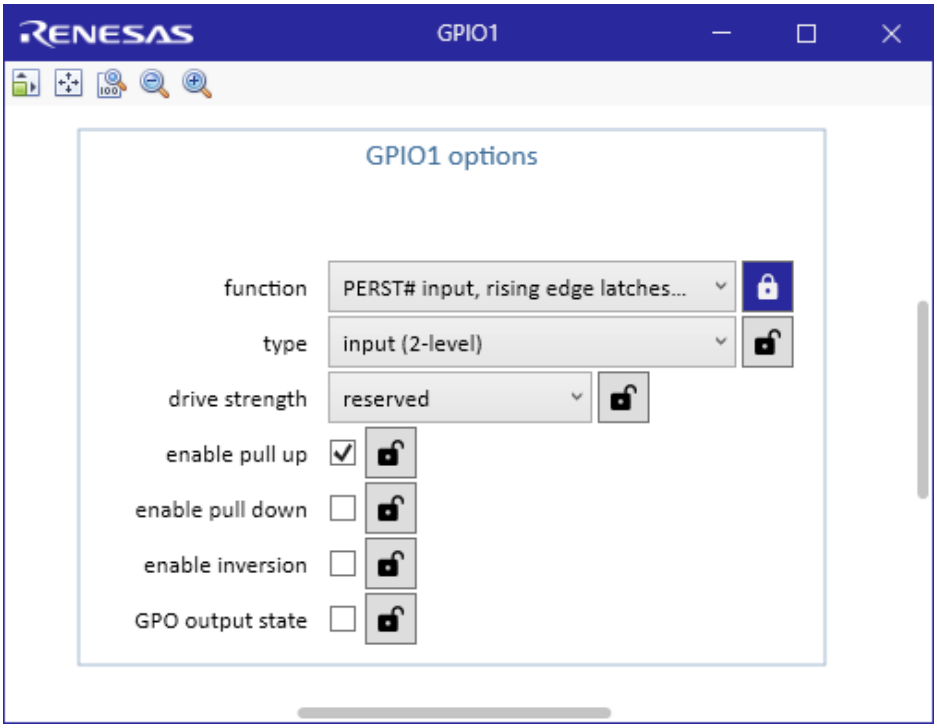
At this point in the setup, the frequency counter should be measuring 100MHz.

1.5.5 Setting Up GPIO for LOS/PERST#

Automatic clock switching between an output divider and a CLKIN is controlled by the state of the LOS signal. When LOS is high, then the output divider is sent to OUT10. When LOS is low, then CLKIN is fanout to OUT10. However, this switch only happens when the PERST# signal is toggled low to high. Only then will the state of LOS determine which clock source is sent to OUT10. By holding PERST# low, the presence of CLKIN will determine which source will be routed to OUT10.

1. Click on the GPIO button to bring up the sub-diagram window.
2. Next click on GPIO0. Set the function to be clkin0_los_sts.
3. Close the GPIO0 sub-diagram window. Since GPIO0 is an output, it is best to set the EVB dip switch to the middle position for GPIO0.
4. Finally, click on GPIO1. Set the function to be PERST#. Use the dip switch to pull the input signal low so that automatic switching can occur. Note that the internal pull-up for GPIO1 is enabled.





2. Testing the Setup

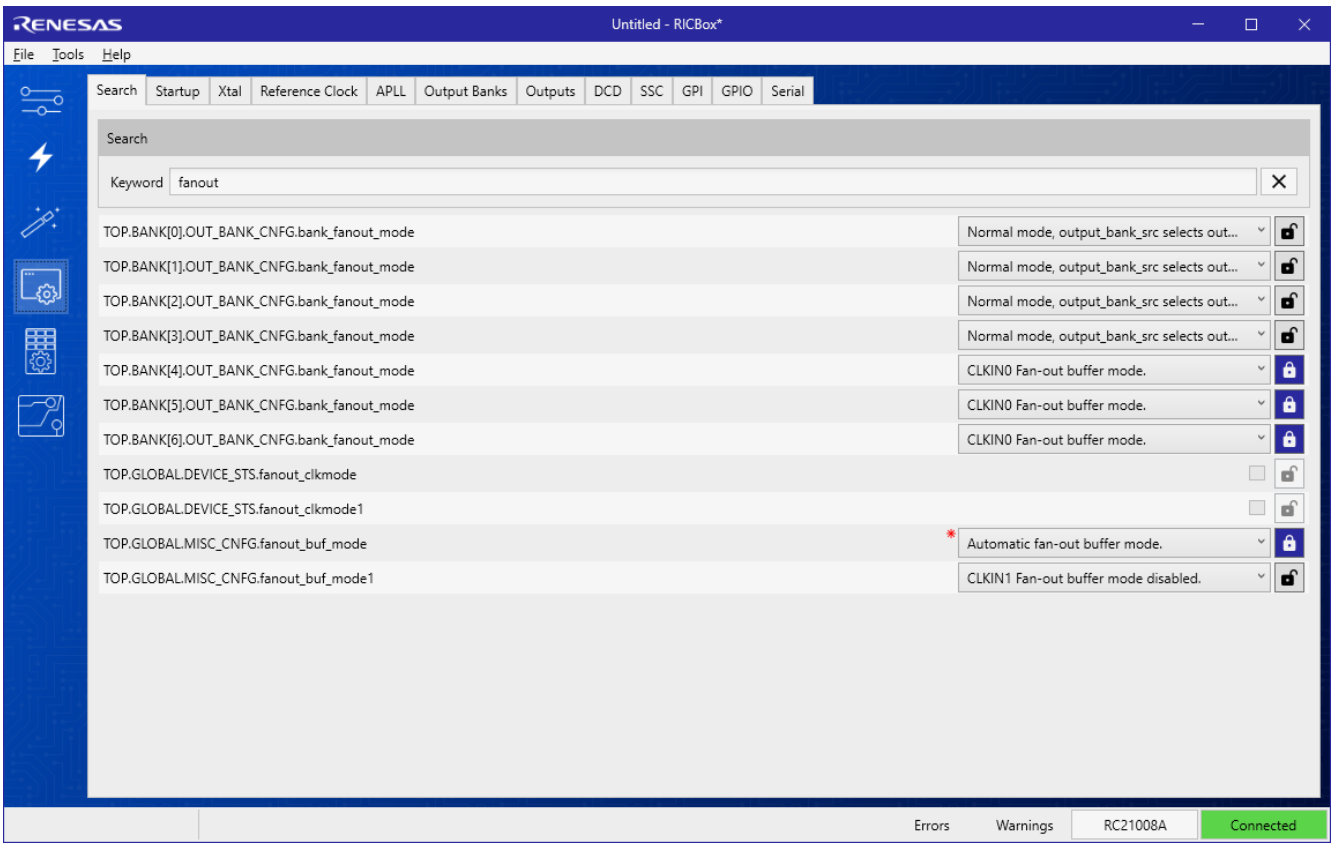
To start testing the setup, place GPIO0 and GPIO1 dip switches in the middle position. The GPIO0 LED should be off. The GPIO1 LED should be on.

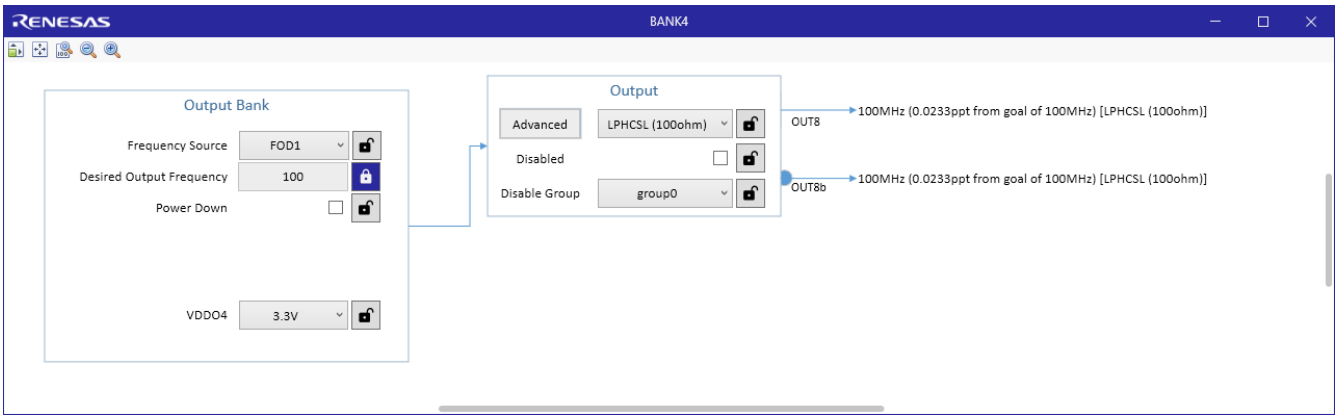
1. Turn the CLKIN signal generator OFF to ensure that the LOS output signal goes high.
2. Turn the CLKIN signal generator ON to ensure the LOS output signal goes low.
3. Turn off the CLKIN signal generator (GPIO0 goes high).
4. Pull GPIO1 (PERST#) low. Confirm with the frequency counter that OUT10 is present.
5. Now turn on the CLKIN signal generator. The switch has now occurred. To verify this, simply change CLKIN frequency to 100.001MHz. OUT10 frequency should reflect this.
6. Finally, turn off the CLKIN signal generator. The automatic switch will occur.

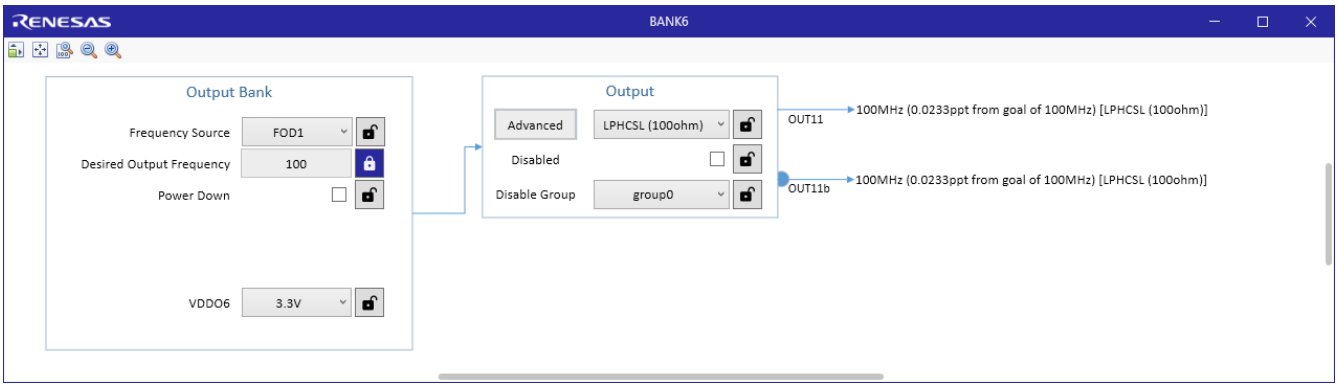
OUT10 will now use the output divider designated in the Bank 5 sub-diagram window. Turning the CLKIN signal generator back on will cause an automatic switch back to CLKIN being fanout to OUT10.

2.1 Enabling Other Banks

To enable the other banks, update the bits-sets for **TOP.BANK[4].OUT_BANK_CNFG.bank_fanout_mode** and **TOP.BANK[6].OUT_BANK_CNFG.bank_fanout_mode** to be CLKIN0 fanout buffer mode, then open up Bank4 and Bank6 sub-diagram windows and enter 100MHz in the desired output frequency field(s).



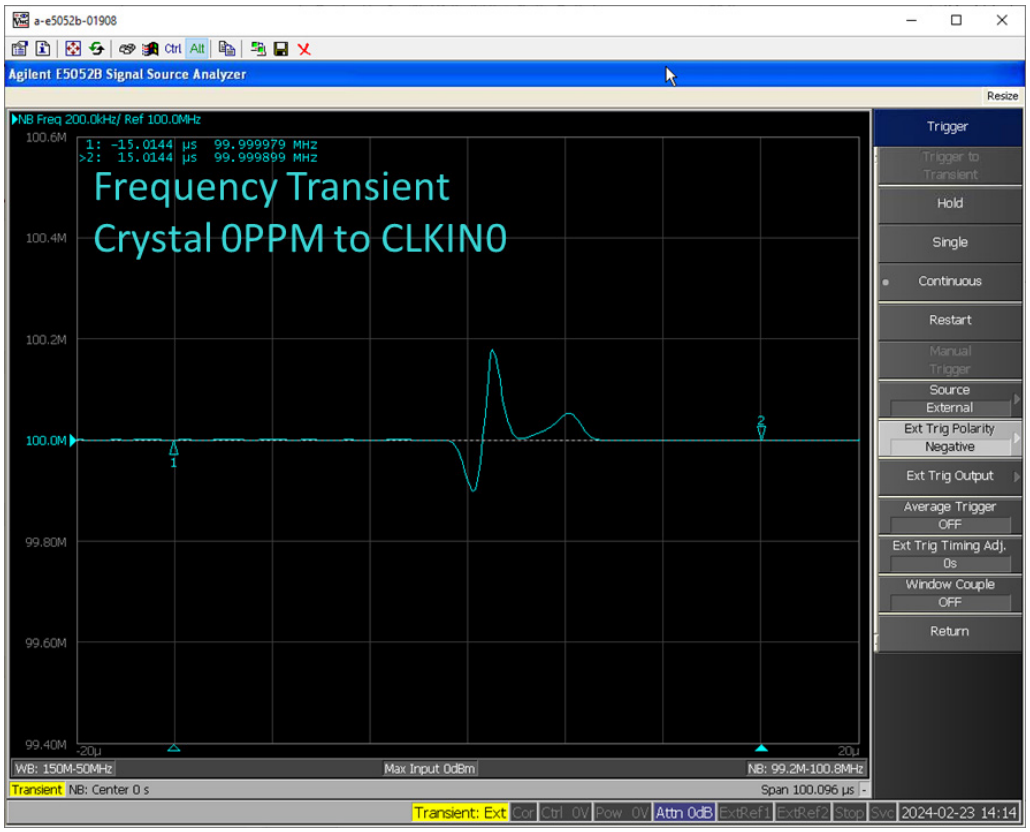

RENESAS
BANK4
Output Bank
Frequency Source
FOD1
Desired Output Frequency
100
Power Down
VDDO4
3.3V
Output
Advanced
LPHCSL (100ohm)
Disabled
Disable Group
group0
OUT8
100MHz (0.0233ppt from goal of 100MHz) [LPHCSL (100ohm)]
OUT8b
100MHz (0.0233ppt from goal of 100MHz) [LPHCSL (100ohm)]


RENESAS
BANK6
Output Bank
Frequency Source
FOD1
Desired Output Frequency
100
Power Down
VDDO6
3.3V
Output
Advanced
LPHCSL (100ohm)
Disabled
Disable Group
group0
OUT11
100MHz (0.0233ppt from goal of 100MHz) [LPHCSL (100ohm)]
OUT11b
100MHz (0.0233ppt from goal of 100MHz) [LPHCSL (100ohm)]

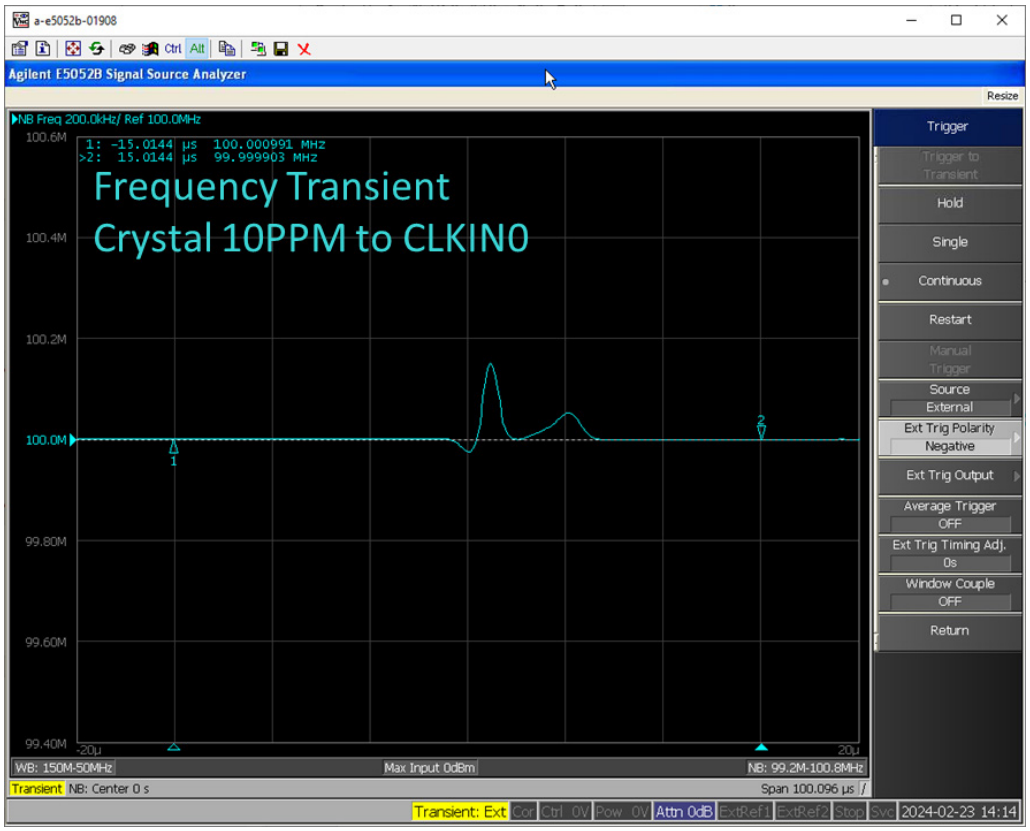
3. Transient Measurements

The following transient measurements display the frequency of OUT10 before and after the transition. The CLKIN0 LOS GPIO was used to trigger the E5052B. The plots show the transitions going from crystal to clkin source and clkin to crystal source. The crystal frequency will be skew by 0 PPM, 10 PPM, and 25 PPM.

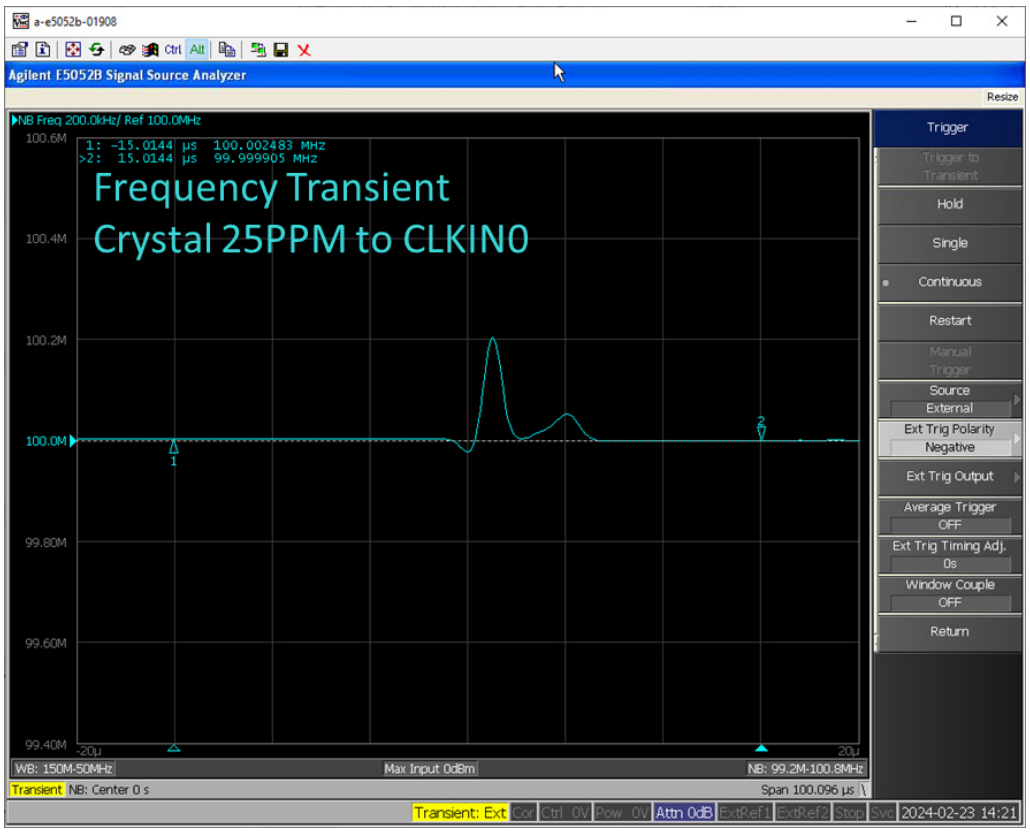
3.1 Crystal 0PPM to CLKIN0



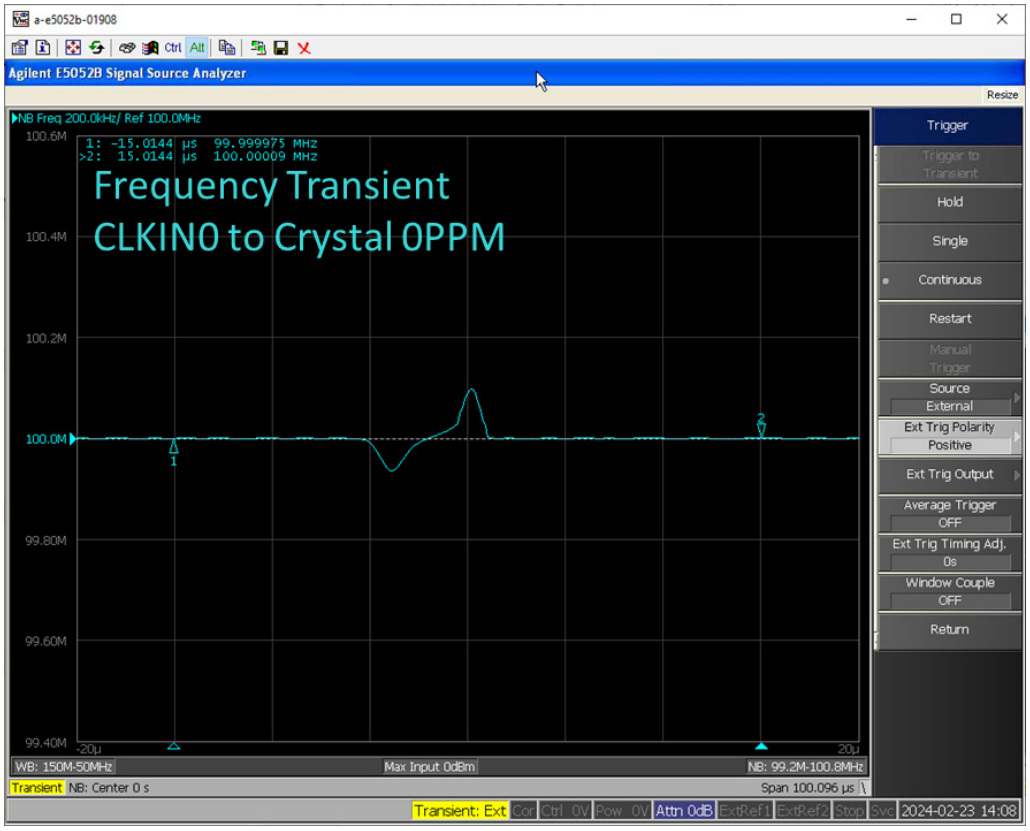
3.2 Crystal 10PPM to CLKIN0



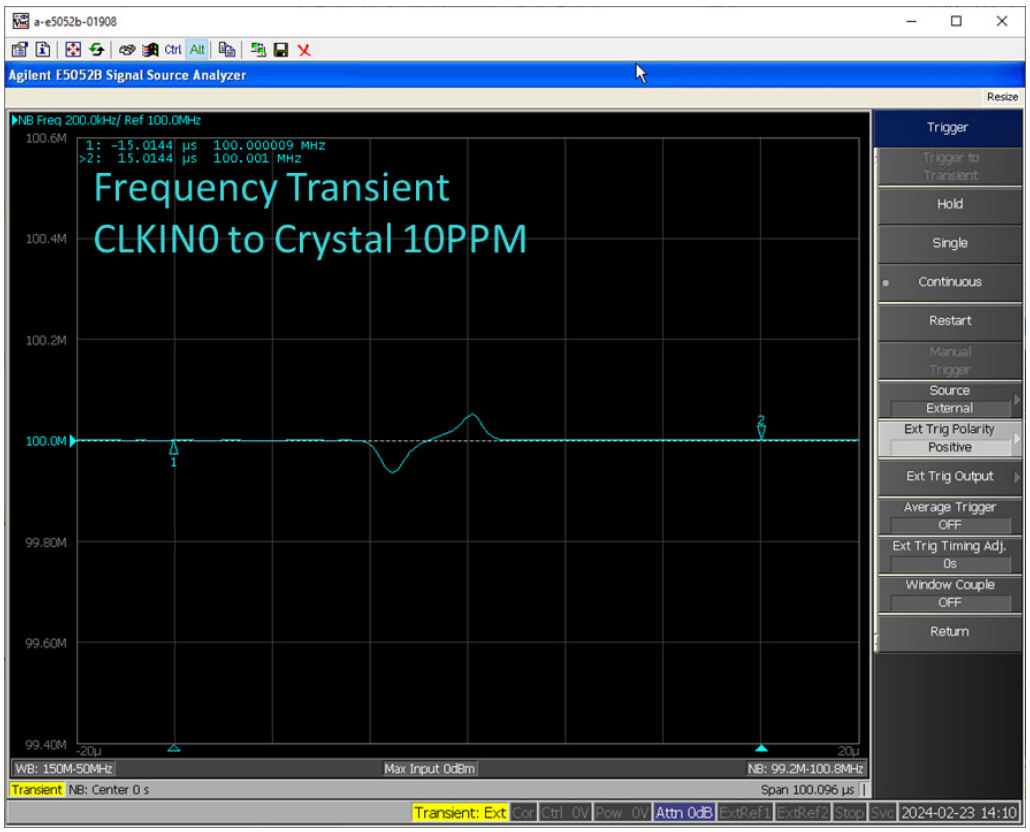
3.3 Crystal 25PPM to CLKIN0



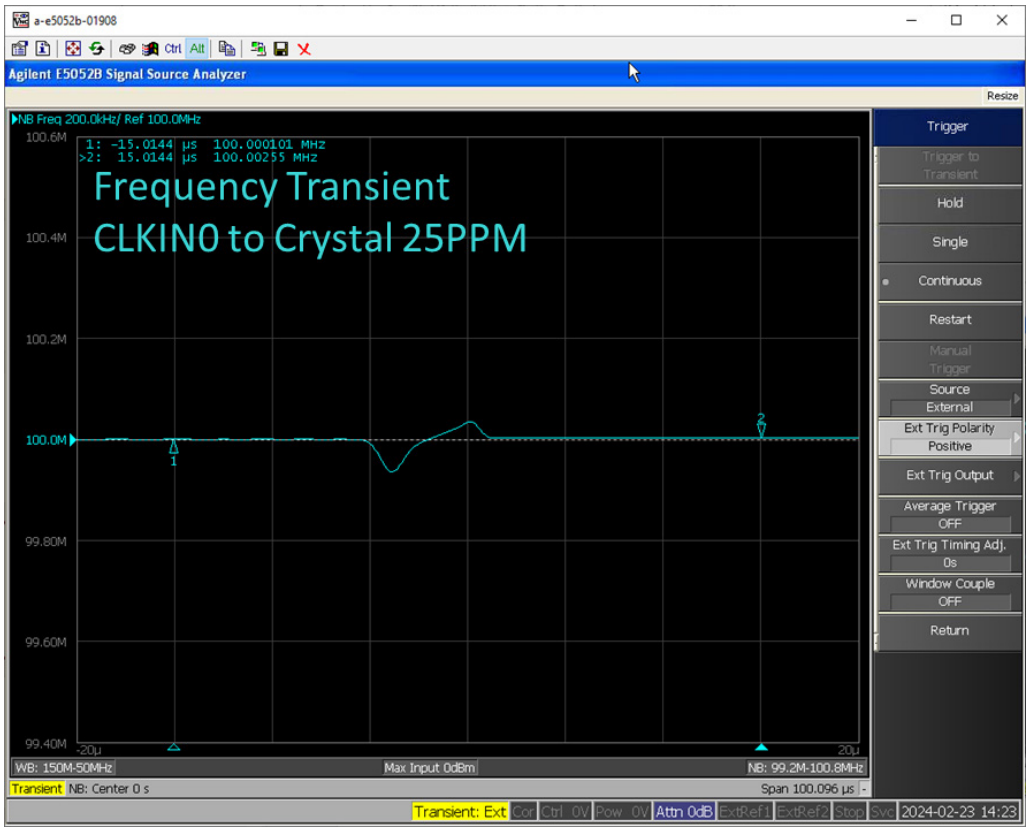
3.4 CLKIN0 to Crystal 0PPM



3.5 CLKIN0 to Crystal 10PPM



3.6 CLKIN0 to Crystal 25PPM



4. Revision History

Revision	Date	Description
1.00	Mar 22, 2024	Initial release.

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