# RENESAS

# VersaClock<sup>®</sup> 7 (VC7) Fanout Buffer Mode for PCI Express

This document describes the steps needed for the Renesas IC Toolbox (RICBox) to enable VC7 to initially output 100MHz using the onboard crystal as the reference, then switch to a CLKIN reference when a GPI/GPIO is toggled (PERST#). Fanout mode is only available for Bank4, Bank5, and Bank6. The RCx1012A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11. The RCx1008A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11. The RCx1008A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11. The RCx1008A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11. The RCx1008A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11. The RCx1008A fanout mode is supported on OUT8, OUT9, OUT10, and OUT11.

# Contents

1.	Ben	ch Setup	p	2
	1.1	Evalua	ation Board (EVB) Setup	2
	1.2	Signal	I Generator Setup	2
	1.3	Freque	ency Counter Setup	2
	1.4	RICBo	ox Installation	2
	1.5	VC7 S	Setup	2
		1.5.1	Trimming the Crystal (optional)	2
		1.5.2	Setting Up CLKIN	4
		1.5.3	Fanout Buffer Mode	5
		1.5.4	Setting Up OUT10	7
		1.5.5	Setting Up GPIO for LOS/PERST#	7
2.	Test	ing the S	Setup	9
	2.1	Enablir	ing Other Banks	
3.	Tran	sient Me	leasurements	11
	3.1	Crysta	al 0PPM to CLKIN0	11
	3.2	Crysta	al 10PPM to CLKIN0	
	3.3	Crystal	al 25PPM to CLKIN0	
	3.4	CLKIN	N0 to Crystal 0PPM	13
	3.5	CLKIN	N0 to Crystal 10PPM	13
	3.6	CLKIN	N0 to Crystal 25PPM	14
4.	Revi	sion His	story	14

# 1. Bench Setup

Equipment used for this measurement are the RC21008A/RC31008A Evaluation Kit (EVK), Signal Generator, and Frequency Counter. The RC21012A/RC31012A EVK may be used as well.



# 1.1 Evaluation Board (EVB) Setup

Rework the evaluation board (EVB) so that CLKIN0 and/or CLKIN1 are connected to VC7. Refer to the <u>RC21008A/RC31008A</u> or <u>RC21012A/RC31012A</u> EVB schematics for more information. For this example, the clock inputs are DC coupled. The clock source will be connected to CLKIN0. GPIO0 and GPIO1 will be used for indicating Loss of Signal (LOS) and PERST#, respectively. Note that PERST1# is also available. Lastly, OUT10 will be connected to the frequency counter. OUT10 is used in this example because the crystal can be muxed out. It is highly recommended that the crystal frequency is trimmed by using external caps on the XIN/XOUT pins or by adjusting TOP.XO.XO\_CNFG register fields en\_cap\_x1 and en\_cap\_x2.

# 1.2 Signal Generator Setup

Any of the accepted clock input types for VC7 can be used to setup the signal generator. Depending on the clock input type, adjust termination on the board or internally using RICBox.

# 1.3 Frequency Counter Setup

Setup the counter to accept 100MHz. If the VC7 EVB has AC-coupled outputs, adjust the counter to enable  $50\Omega$  termination.

# **1.4 RICBox Installation**

For more information on installing RICBox software for VC7, see the Renesas IC Toolbox User Guide.

# 1.5 VC7 Setup

Use RICBox to trim the on-board crystal (optional), setup clock input, fanout buffer mode, clock output, and GPIO (LOS/PERST#).

### 1.5.1 Trimming the Crystal (optional)

As previously mentioned, OUT10 will be the output to measure as the crystal signal can be muxed out. This step is optional but highly recommended. Otherwise, large PPM offsets will result in many little spurs in the phase noise plot.

- 1. Start RICBox and create a new project.
- 2. Choose the product variant that matches the unit on the EVB.
- 3. During the wizard phase, simply click Finish.
- 4. View the block diagram. If your crystal is different from the default value, then update the XIN\_REFIN frequency.



### VersaClock 7 (VC7) Fanout Buffer Mode for PCI Express

5. Click on Bank5 to bring up the sub-diagram window. For the *Frequency Source*, choose XIN\_REFIN. Set the *Desired Output Frequency* to match the crystal frequency.

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Output E	Bank	Output		
Frequency Source	XIN_REFIN 🗸 🔒	Advanced LPHCSL (100ohm) v		
Desired Output Frequency	68 🔒	Disabled		
Power Down		Disable Group group0 v o OUT10b		
VDD05	3.3V ~ 🖬			

6. Connect and program VC7. Use the frequency counter to measure the crystal frequency. Go back to the main block diagram and click on the XIN\_REFIN block to bring up the sub-diagram window. Adjust the *Load Capacitance* until the measure frequency by the counter is closest to your expected crystal frequency. Use 0.1 (pF) steps for the best results. After changing the load capacitance value, program VC7 again.

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<b>a</b>	8 Q Q			
	Input	Pad		
	Mode	Xtal	× B	
	Frequency	68MHz	ê	
	Load Capacitance (pF)	11.75	ê	
	Clock Monitor	Div	vider	
	XIN/REFIN	Hdi	iv XO	

7. Close the XIN\_REFIN sub-diagram window and go back to the Bank5 sub-diagram window. Click on the Blue Locks to reset the fields back to the GUI defaults.

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Output	Bank	Output		
Frequency Source	FOD1 v	Advanced powered down v		
Desired Output Frequency	None	Disabled 🗹 🖬		
Power Down		Disable Group group0 v o OUT10b Powered down (HI-2)		
				- 1
VDD05	3.3V ×			

The onboard crystal is now trimmed.

### 1.5.2 Setting Up CLKIN

CLKIN0 or CLKIN1 – or both – may be used for the fanout source. For this example, CLKIN0 will be used. The following steps can also be applied to CLKIN1:

- 1. Start by setting the CLKIN0 frequency to 100MHz.
- 2. Push the CLKIN0 button to open up the sub diagram window.
- 3. Choose the appropriate mode to match your clock input type.
- 4. Close the CLKIN0 sub-diagram window when completed.



#### VersaClock 7 (VC7) Fanout Buffer Mode for PCI Express

#### 1.5.3 Fanout Buffer Mode

1. On the left of the RICBox window, click on the Configuration icon to view all the fields and register bit-sets.

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<u> </u>	Search Startup Xtal Reference Clock APLL Output Banks Outputs DCD SSC GPI GPIO Serial		
	Search		
7	Keyword		×
p.	addendum version	v1.0	<b>_</b>
	apll_divider_ratio	~73.5294	
டஞ்ச	apll_freq_actual	10GHz	<b>D</b>
Configurat	ion bll_freq_goal	10GHz	6
<u>fô</u>	apll_input_freq	68MHz	
F-72	apll_pfd_input_freq	136MHz	
드외	auto_write		
	config_slot_0		~ <b>6</b>
	config_slot_1		~ <b>6</b>
김리카	config_slot_2		~ <b>d</b>
7 <u>/</u> 1176	config_slot_3		~ E
	config_slot_4		~ <b>S</b>
	config_slot_5		~ E
	config_slot_6		~ <b>E</b>
))[]/	config_slot_7		× B
	config_slot_8		~ <b>E</b>
크게뜨	config slot 0		~
		Errors Warnings RC21008A	Connected

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2. In the search field near the top, type in "fanout" and push enter.

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<u> </u>	Search	Startup	Xtal	Reference Clock	APLL	Output Banks	Outputs	DCD	SSC	GPI G	PIO	Serial						IJĘ
4	Sear Key	:h vord fanc	ut														×	:
je:	TOP.	ANK[0].OU	BANK	(_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	ts out	~	ſ
	TOP.	ANK[1].OU		_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	s out	× 1	ſ
டஞ	TOP.	ANK[2].OU	T_BANK	_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	ts out	۲	ſ
<b>⊞</b>	TOP.	ANK[3].OU	T_BANK	_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	ts out	× (	ſ
<u>نې</u>	TOP.	ANK[4].OU	T_BANK	_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	s out	× (	ſ
F-21	TOP.E	ANK[5].OU	T_BANK	_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	s out	× (	ſ
닫외	TOP.	ANK[6].OU	T_BANK	_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src select	ts out	× (	ſ
	TOP.0	GLOBAL.DE	/ICE_ST	S.fanout_clkmode														ſ
	TOP.0	GLOBAL.DE	/ICE_ST	5.fanout_clkmode1												[		ſ
2 FUL	TOP.0	GLOBAL.MIS	SC_CNF	5.fanout_buf_mode	2									CLKIN0 Fan-out	buffer mode disabled	l.	× (	ſ
	TOP.0	GLOBAL.MIS	C_CNF	3.fanout_buf_mode	e1									CLKIN1 Fan-out	buffer mode disabled	l.	× (	ſ
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- 3. Bank4, Bank5, and Bank6 support fan-out buffer mode. OUT10 (Bank5) will be used for this example. As a result, the register field **TOP.BANK[5].OUT\_BANK\_CNFG.bank\_fanout\_mode** will need to be updated to select CLKIN0 fanout buffer mode.
- 4. Next, update **TOP.GLOBAL.MISC\_CNFG.fanout\_buf\_mode** to *Automatic fan-out buffer mode*.

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	Search	Startup	Xtal	Reference Clock	APLL	Output Banks	Outputs	DCD	SSC	GPI	GPIO	Serial						
4	Search																	
	Keywo	ord fano	ut															×
p.	TOP.BA	NK[0].OU	T_BANK	_CNFG.bank_fanc	ut_mode									Normal mode, o	output_bank_s	src selects c	ut ~	đ
	TOP.BA	NK[1].OU	T_BANK	_CNFG.bank_fanc	ut_mode									Normal mode, o	output_bank_	src selects c	out ~	đ
L	TOP.BA	NK[2].OU	T_BANK	_CNFG.bank_fanc	ut_mode									Normal mode, o	output_bank_	src selects o	ut ~	đ
<b>E</b>	TOP.BA	NK[3].OU	T_BANK	_CNFG.bank_fanc	ut_mode									Normal mode, o	output_bank_s	src selects c	out ~	đ
[ <u>[</u> ]	TOP.BA	NK[4].OU	T_BANK	_CNFG.bank_fanc	ut_mode									Normal mode, o	output_bank_	src selects o	out ~	
	TOP.BA	NK[5].OU	T_BANK	_CNFG.bank_fand	ut_mode									CLKIN0 Fan-out	buffer mode		Ý	â
	TOP.BA	NK[6].OU	T_BANK	_CNFG.bank_fanc	ut_mode									Normal mode, o	output_bank_s	src selects o	out ~	đ
	TOP.GI	.OBAL.DE\	/ICE_STS	S.fanout_clkmode														
	TOP.GI	.OBAL.DE\	/ICE_STS	S.fanout_clkmode	1													
	TOP.GI	.OBAL.MIS	C_CNFC	5.fanout_buf_mod	e									Automatic fan-c	out buffer mo	de.	~	â
	TOP.GI	OBAL.MIS	C_CNFC	3.fanout_buf_mod	e1									CLKIN1 Fan-out	buffer mode	disabled.	Ý	đ
득기년									_									
													Errors	Warnings	RC210	08A	Conn	ected

#### 1.5.4 Setting Up OUT10

Click on the block diagram icon on the left side of RICBox window to display the main block diagram again. Click on Bank5 button to bring up the sub-diagram window.

- 1. Enter the desired output frequency (100MHz).
- 2. Choose the appropriate output type.
- 3. Close the sub-diagram window when completed.

RENESAS	BANKS –	×
i 🔁 🗟 🍭 🔍		
Output Bank	Output > 100MHz (0.0233ppt from goal of 100MHz) [LPHCSL (100ohm)]	
Frequency Source FOD1	Advanced LPHCSL (100ohm) V	
Desired Output Frequency 100MHz 6	Disabled Disabled	
Power Down	Disable Group group0 v of OUT10b	
VDD05 3.3V ~		

At this point in the setup, the frequency counter should be measuring 100MHz.

### 1.5.5 Setting Up GPIO for LOS/PERST#

Automatic clock switching between an output divider and a CLKIN is controlled by the state of the LOS signal. When LOS is high, then the output divider is sent to OUT10. When LOS is low, then CLKIN is fanout to OUT10. However, this switch only happens when the PERST# signal is toggled low to high. Only then will the state of LOS determine which clock source is sent to OUT10. By holding PERST# low, the presence of CLKIN will determine which source will be routed to OUT10.

- 1. Click on the GPIO button to bring up the sub-diagram window.
- 2. Next click on GPIO0. Set the function to be clkin0\_los\_sts.
- 3. Close the GPIO0 sub-diagram window. Since GPIO0 is an output, it is best to set the EVB dip switch to the middle position for GPIO0.
- 4. Finally, click on GPIO1. Set the function to be PERST#. Use the dip switch to pull the input signal low so that automatic switching can occur. Note that the internal pull-up for GPIO1 is enabled.

RE	NESAS	GPIO0	_		×
<b>i</b> -	· []\$ Q Q				
		GPIO0 options			
	function type drive strength	clkin0 los_sts output output (high/low), or bidirectional	> >	<b>6</b>	
	enable pull up enable pull down enable inversion GPO output state				

RENESAS	GPIO1	—		×
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	GPIO1 options			
function	PERST# input, rising edge latches	~	ê	
type	input (2-level)	~	Ð	
drive strength	reserved ~			
enable pull up				
enable pull down				1
enable inversion				
GPO output state				

# 2. Testing the Setup

To start testing the setup, place GPIO0 and GPIO1 dip switches in the middle position. The GPIO0 LED should be off. The GPIO1 LED should be on.

- 1. Turn the CLKIN signal generator OFF to ensure that the LOS output signal goes high.
- 2. Turn the CLKIN signal generator ON to ensure the LOS output signal goes low.
- 3. Turn off the CLKIN signal generator (GPIO0 goes high).
- 4. Pull GPIO1 (PERST#) low. Confirm with the frequency counter that OUT10 is present.
- 5. Now turn on the CLKIN signal generator. The switch has now occurred. To verify this, simply change CLKIN frequency to 100.001MHz. OUT10 frequency should reflect this.
- 6. Finally, turn off the CLKIN signal generator. The automatic switch will occur.

OUT10 will now use the output divider designated in the Bank 5 sub-diagram window. Turning the CLKIN signal generator back on will cause an automatic switch back to CLKIN being fanout to OUT10.

### 2.1 Enabling Other Banks

To enable the other banks, update the bits-sets for **TOP.BANK[4].OUT\_BANK\_CNFG.bank\_fanout\_mode** and **TOP.BANK[6].OUT\_BANK\_CNFG.bank\_fanout\_mode** to be CLKIN0 fanout buffer mode, then open up Bank4 and Bank6 sub-diagram windows and enter 100MHz in the desired output frequency field(s).

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<u>F</u> ile <u>T</u> ools	<u>H</u> elp	- / * -										/ •		/ •				
<u> </u>	Search	Startup	Xtal	Reference Clock	APLL	Output Banks	Outputs	DCD	SSC G	PI GP	O Seri	al						
4	Search																	
	Keyword fanout													×	:			
10.	TOP.B4	NK[0].OU	T_BANK	CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src selec	ts out	× I	ſ
	TOP.B4	NK[1].OU	T_BANK	<pre>CNFG.bank_fanot</pre>	ut_mode									Normal mode, o	utput_bank_src selec	ts out	× I	ſ
டலு	TOP.B4	NK[2].OU	T_BANK	CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src selec	ts out	× 1	ſ
E	TOP.B4	NK[3].OU	T_BANK	(_CNFG.bank_fanou	ut_mode									Normal mode, o	utput_bank_src selec	ts out	× I	ſ
<u>{</u>	TOP.B4	NK[4].OU	T_BANK	CNFG.bank_fanou	ut_mode									CLKIN0 Fan-out	buffer mode.		~	â
27	TOP.B4	NK[5].OU	T_BANK	CNFG.bank_fanou	ıt_mode									CLKIN0 Fan-out	buffer mode.		~	â
	TOP.B4	NK[6].OU	T_BANK	K_CNFG.bank_fanou	ut_mode									CLKIN0 Fan-out	buffer mode.		~	â
플인브	TOP.GI	.OBAL.DE\	/ICE_ST	S.fanout_clkmode														n l
	TOP.GI	.OBAL.DE\	/ICE_ST	S.fanout_clkmode1												[		n l
27U	TOP.GI	.OBAL.MIS	C_CNF	G.fanout_buf_mode									*	Automatic fan-o	ut buffer mode.		~	â
<u>74</u> 11	TOP.GI	OBAL.MIS	SC_CNF	G.fanout_buf_mode	1									CLKIN1 Fan-out	buffer mode disabled	d.	۲	ſ
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<b>a</b>	. 🕼 q. q										
	Output	Bank		] [		Output		100MHz /0.0222ppt from a	and of 100MHz) [I PHCSI (10	(Oohm)]	
	Frequency Source	FOD1	ř		Advanced	LPHCSL (100ohm) 👋	ſ	OUT11	0810110000112/[EFTIC3E (10	oonni)	
	Desired Output Frequency	100	ê		Disabled		î	>100MHz (0.0233ppt from e	oal of 100MHz) [IPHCSI (10	0ohm)]	1
	Power Down				Disable Group	group0 ~	ĵ	OUT11b		001111/]	
											_
	VDDO6	3.3V	ř								

# 3. Transient Measurements

The following transient measurements display the frequency of OUT10 before and after the transition. The CLKIN0 LOS GPIO was used to trigger the E5052B. The plots show the transitions going from crystal to clkin source and clkin to crystal source. The crystal frequency will be skew by 0 PPM, 10 PPM, and 25 PPM.

# 3.1 Crystal 0PPM to CLKIN0



# 3.2 Crystal 10PPM to CLKIN0



# 3.3 Crystal 25PPM to CLKIN0



# 3.4 CLKIN0 to Crystal 0PPM



# 3.5 CLKIN0 to Crystal 10PPM





# 3.6 CLKIN0 to Crystal 25PPM



# 4. Revision History

Revision	Date	Description
1.00	Mar 22, 2024	Initial release.

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TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

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