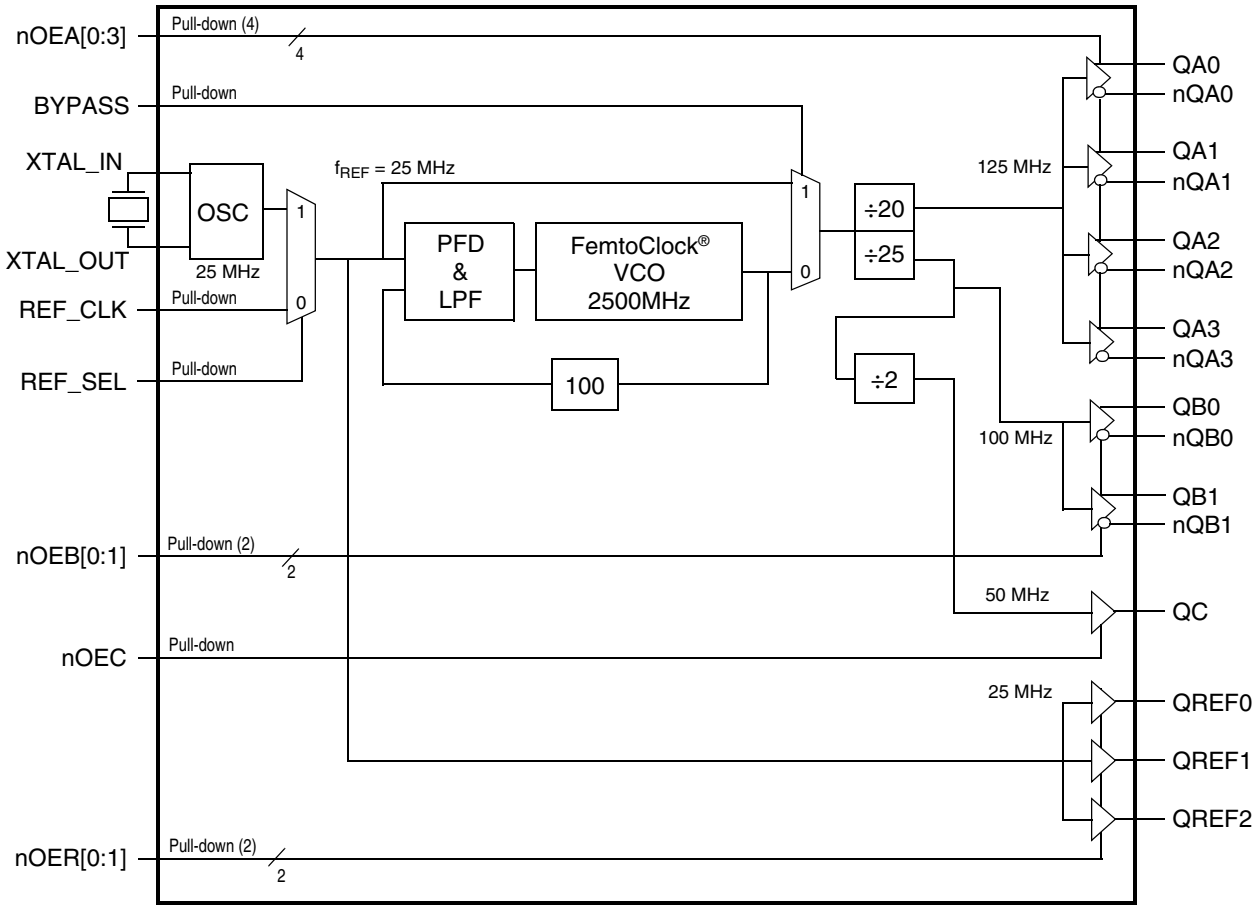
General Description

The 8V44S269 is a ten LVDS/LVTTL output clock synthesizer designed for instrumentation and wireless applications. The device generates four copies of a 125MHz, two copies of a 100MHz differential LVDS clock and one 50MHz (LVCMOS) signal with excellent phase jitter performance. The PLL is optimized for a reference frequency of 25MHz. Both a crystal interface and a single-ended input are supported for the reference frequency. Three LVCMOS outputs duplicate the reference frequency and are provided for clock tree cascade purpose. Each of the four LVCMOS outputs can be supplied with either 3.3V, 2.5V or 1.8V, forming the respective LVCMOS output levels of 3.3V, 2.5V or 1.8V. The device uses IDT's third generation FemtoClock® technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption. The device supports a 3.3V voltage supply and is packaged in a small, lead-free (RoHS 6) 48-lead VFQFN package.

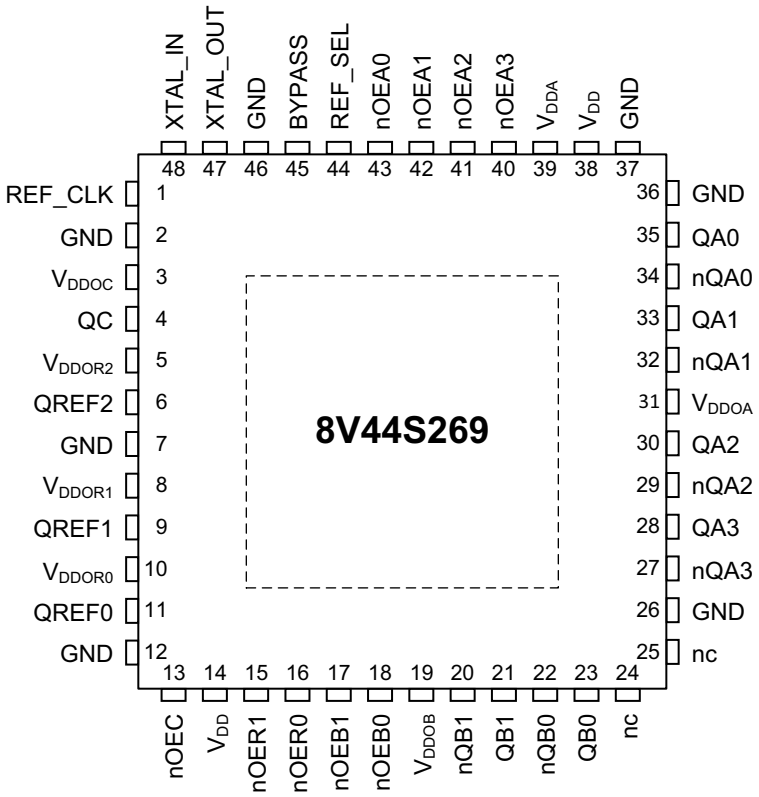
Features

- Third generation FemtoClock® technology
- 125MHz, 100MHz and 50MHz output clocks synthesized from a 25MHz reference clock or fundamental mode crystal
- Six differential LVDS clock outputs
- QA[0:3] outputs (125MHz) are LVDS compatible
- QB[0:1] outputs (100MHz) are LVDS compatible
- Four single-ended LVCMOS-compatible reference clock outputs
- QC output (50MHz) is LVCMOS 3.3V, 2.5V or 1.8V compatible
- QREF[0:2] (25MHz) are LVCMOS 3.3V, 2.5V or 1.8V compatible
- Crystal interface designed for 25MHz XTAL
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz - 20MHz): 0.57 (typical)
- RMS phase jitter @ 100MHz, using a 25MHz crystal (12kHz - 20MHz): 0.58 (typical)
- LVCMOS interface levels for the control input
- I/O supply voltages for LVDS:
  Core/Output
  3.3V/2.5V
- I/O supply voltages for LVCMOS:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
- Lead-free (RoHS 6) 48-lead VFQFN packaging
- -55°C to 105°C ambient operating temperature

Block Diagram



Pin Assignment



Pin Description and Characteristic Tables

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	REF_CLK	Input	Pull-down	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
2	GND	Power		Ground power supply (0V).
3	V_{DDOC}	Power		Output supply for the QC output.
4	QC	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
5	V_{DDOR2}	Power		Output supply for the QREF2 output.
6	QREF2	Output		Single-ended clock output (copy 2 of the reference clock). LVCMOS/LVTTL interface levels.
7	GND	Power		Ground power supply (0V).
8	V_{DDOR1}	Power		Output supply for the QREF1 output.
9	QREF1	Output		Single-ended clock output (copy 1 of the reference clock). LVCMOS/LVTTL interface levels.
10	V_{DDOR0}	Power		Output supply for the QREF0 output.
11	QREF0	Output		Single-ended clock output (copy 0 of the reference clock). LVCMOS/LVTTL interface levels.
12	GND	Power		Ground power supply (0V).

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
13	nOEC	Input	Pull-down	Output enable inputs for the individual QC output. See Table 3E on page 6 for function. LVCMOS/LVTTL interface levels.
14	V_{DD}	Power		Core supply.
15	nOER1	Input	Pull-down	Output enable inputs for the QREF2 output. See Table 3F on page 6 for function. LVCMOS/LVTTL interface levels.
16	nOER0	Input	Pull-down	Output enable inputs for the QREF[0:1] outputs. See Table 3F on page 6 for function. LVCMOS/LVTTL interface levels.
17	nOEB1	Input	Pull-down	Output enable inputs for the QB1 output. See Table 3D on page 6 for function. LVCMOS/LVTTL interface levels.
18	nOEB0	Input	Pull-down	Output enable inputs for the QB0 output. See Table 3D on page 6 function. LVCMOS/LVTTL interface levels.
19	V_{DDOB}	Power		Output supply for the Bank B outputs.
20	nQB1	Output		Inverted differential clock output pair. LVDS interface levels.
21	QB1	Output		Non-inverted Differential clock output pair. LVDS interface levels.
22	nQB0	Output		Inverted differential clock output pair. LVDS interface levels.
23	QB0	Output		Non-inverted Differential clock output pair. LVDS interface levels.
24	nc	Unused		No internal connection.
25	nc	Unused		No internal connection.
26	GND	Power		Ground power supply (0V).
27	nQA3	Output		Inverted differential clock output pair. LVDS interface levels.
28	QA3	Output		Non-inverted Differential clock output pair. LVDS interface levels.
29	nQA2	Output		Inverted differential clock output pair. LVDS interface levels.
30	QA2	Output		Non-inverted Differential clock output pair. LVDS interface levels.
31	V_{DDOA}	Power		Output supply for the Bank A outputs.
32	nQA1	Output		Inverted differential clock output pair. LVDS interface levels.
33	QA1	Output		Non-inverted Differential clock output pair. LVDS interface levels.
34	nQA0	Output		Inverted differential clock output pair. LVDS interface levels.
35	QA0	Output		Non-inverted Differential clock output pair. LVDS interface levels.
36	GND	Power		Ground power supply (0V).
37	GND	Power		Ground power supply (0V).
38	V_{DD}	Power		Core supply.
39	V_{DDA}	Power		Analog power supply.
40	nOEA3	Input	Pull-down	Output enable inputs for the QA3 output. See Table 3C on page 6 for function. LVCMOS/LVTTL interface levels.
41	nOEA2	Input	Pull-down	Output enable inputs for the QA2 output. See Table 3C on page 6 for function. LVCMOS/LVTTL interface levels.

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
42	nOEA1	Input	Pull-down	Output enable inputs for the QA1 output. See Table 3C on page 6 for function. LVCMOS/LVTTL interface levels.
43	nOEA0	Input	Pull-down	Output enable inputs for the QA0 output. See Table 3C on page 6 for function. LVCMOS/LVTTL interface levels.
44	REF_SEL	Input	Pull-down	Reference select. See Table 3A on page 6 for function. LVCMOS/LVTTL interface levels.
45	BYPASS	Input	Pull-down	PLL bypass mode select. See Table 3B on page 6 for function. LVCMOS/LVTTL interface levels.
46	GND	Power		Ground power supply (0V).
47	XTAL_OUT	Crystal Output		Crystal Output. Crystal oscillator interface.
48	XTAL_IN	Crystal Input		Crystal Input. Crystal oscillator interface.
—	Exposed Pad	Ground		Ground power supply (0V). The exposed pad is a ground return path of the circuit and requires a connection to 0V.

NOTE 1. Pull-down refers to internal input resistors. See Table 2, "Pin Characteristics".

Table 2. Pin Characteristics[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	REF_CLK, nOEA[0:3], nOEB[0:1], nOEC, nOER[0:1], REF_SEL, BYPASS			2		pF
$R_{PULLDOWN}$	Input Pull-down Resistor				51		kΩ
R_{OUT}	Output Impedance		QREF[0:2], QC, V_{DDOn} = 3.3V		18		Ω
			QREF[0:2], QC, V_{DDOn} = 2.5V		23		Ω
			QREF[0:2], QC, V_{DDOn} = 1.8V		35		Ω

NOTE 1. V_{DDOn} denotes V_{DDOC}, V_{DDOR0}, V_{DDOR1}, V_{DDOR2}.

Function Tables

Table 3A. PLL Reference Clock Select Function Table[1]

Input REF_SEL	Operation
0 (default)	The REF_CLK input is selected as reference clock
1	The crystal interface is selected as reference clock

NOTE 1. REF_SEL is an asynchronous control input.

Table 3B. PLL Bypass Select Function Table[1]

Input BYPASS	Operation
0 (default)	PLL mode
1	PLL bypass mode. The reference clock is routed to the output dividers. AC specifications do not apply in PLL bypass mode.

NOTE 1. BYPASS is an asynchronous control input.

Table 3C. Outputs QA[0:3] Enable Function Table[1]

Input nOEAn	Operation
0 (default)	Output QAn, nQAn is enabled
1	Output QAn, nQAn is disabled in high-impedance state

NOTE 1. n = 0 to 3.
Each QAn, nQAn output is individually controlled by the corresponding nOEAn input. nOEAn are asynchronous control inputs.

Table 3D. Outputs QB[0:1] Enable Function Table[1]

Input nOEBn	Operation
0 (default)	Outputs QBn, nQBn are enabled
1	Outputs QBn, nQBn are disabled in high-impedance state

NOTE 1. n = 0 to 1.
Each QBn, nQBn output is individually controlled by the corresponding nOEBn input. nOEBn are synchronous control inputs.

Table 3E. Outputs QC Enable Function Table[1]

Input nOEC	Operation
0 (default)	Output QC is enabled
1	Output QC is disabled in high-impedance state

NOTE 1. nOEC is an asynchronous control input.

Table 3F. Outputs QREF[0:2] Enable Function Table[1]

Input		Operation	
nOER0	nOER1	Outputs QREF[0:1]	Output QREF2
0 (default)	0 (default)	Enabled	Enabled
0	1	Enabled	Disabled in high-impedance state
1	0	Disabled in high-impedance state	Enabled
1	1	Disabled in high-impedance state	Disabled in high-impedance state

NOTE 1. nOER[0:1] are asynchronous control inputs.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DDOn}[1] + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Storage Temperature, T_{STG}	-65°C to 150°C
Junction Temperature, T_J	125°C

NOTE 1. V_{DDOn} denotes V_{DDOC}, V_{DDOR0}, V_{DDOR1}, V_{DDOR2}.

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics,

V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, $V_{DDORn,}$[1] V_{DDOC} = (2.5V to 3.3V) ±5%, 1.8V ± 0.2V, T_A = -55°C to 105°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.16	3.3	V_{DD}	V
$V_{DDOA, B}$	LVDS Output Supply Voltage		2.375	2.5	2.625	V
V_{DDOR0}, V_{DDOR1}, V_{DDOR2}, V_{DDOC}	LVCMOS Output Supply Voltage[2]		1.6	1.8	2.0	V
			2.375	2.5	2.625	V
			3.135	3.3	3.465	V
I_{DD}	Core Supply Current			80	91	mA
I_{DDA}	Analog Supply Current			12	16	mA
I_{DDOA} + I_{DDOB}	LVDS Output Supply Current			122	137	mA
I_{DDORn}[3] + I_{DDOC}	LVCMOS Output Power Current	QC, QREF[0:2]; No External Load		2	3	mA

NOTE 1. V_{DDOn} denotes V_{DDOR0}, V_{DDOR1}, V_{DDOR2}.

NOTE 2. Each V_{DDORn} (n = 0 to 2) and V_{DDOC} voltage may be left open, connected to GND or supplied by 1.8V, 2.5V or 3.3V.

NOTE 3. I_{DDORn} denotes I_{DDOR0}, I_{DDOR1}, I_{DDOR2}.

Table 5B. LVCMOS/LVTTL DC Characteristics,
V_{DD} = 3.3V±5%, V_{DDORn},[1] V_{DDOC} = (2.5V to 3.3V) ±5%, 1.8V ± 0.2V, T_A = -55°C to 105°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[2]		V_{DD} = 3.3V	2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	REF_SEL, nOEA[0:3], nOEB[0:1], nOER[0:1], BYPASS, REF_CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	REF_SEL, nOEA[0:3], nOEB[0:1], nOER[0:1], BYPASS, REF_CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage[3]	QC, QREF[0:2]	V_{DDOn}[4] = 3.465V	2.6			V
			V_{DDOn}[4] = 2.625V	1.8			V
			V_{DDOn}[4] = 2V	1.5			V
V_{OL}	Output Low Voltage[3]	QC, QREF[0:2]	V_{DDOn}[4] = 3.465V			0.5	V
			V_{DDOn}[4] = 2.625V			0.5	V
			V_{DDOn}[4] = 2V			0.4	V

NOTE 1. V_{DDORn} denotes V_{DDOR0}, V_{DDOR1}, V_{DDOR2}.
NOTE 2. nOEA[0:3], nOEB[0:1], nOER[0:1], nOEC, BYPASS and REF_CLK inputs are 3.3V tolerant.
NOTE 3. Output terminated with 50Ω to V_{DD}/ 2. See Section, "Parameter Measurement Information".
NOTE 4. V_{DDOn} denotes V_{DDOC}, V_{DDOR0}, V_{DDOR1}, V_{DDOR2}.

Table 5C. LVDS DC Characteristics, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, T_A = -55°C to 105°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		488	mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage		0.975		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF
Capacitive Loading (C_L)			12		pF

AC Electrical Characteristics

Table 7. AC Characteristics,
V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, V_{DDORn},[1] V_{DDOC} = (2.5V to 3.3V) ±5%, 1.8V ± 0.2V, T_A = -55°C to 105°C[2, 3]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency		BYPASS = 0		2500		MHz
f_{OUT}	Output Frequency, QA[0:3]				125		MHz
	Output Frequency, QB[0:1]				100		MHz
	Output Frequency, QC				50		MHz
	Output Frequency, QREF[0:2]				25		MHz
f_{REF}	Reference Frequency				25		MHz
$t_{jit}(Ø)$	RMS Phase Jitter (Random)	QA[0:3]	f_{OUT} = 125MHz, Integration Range: 12kHz – 20MHz		0.57	0.8	ps
		QB[0:1]	f_{OUT} = 100MHz, Integration Range: 12kHz – 20MHz		0.58	0.8	ps
		QC	f_{OUT} = 50MHz, Integration Range: 12kHz – 20MHz		0.78	1.20	ps
		QREF[0:2]	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.85	1.32	ps
$Φ_N$(1k)	Single-side Band Phase Noise 100MHz Output Frequency		1kHz Offset from Carrier		-126	-119	dBc/Hz
$Φ_N$(10k)			10kHz Offset from Carrier		-132	-126.9	dBc/Hz
$Φ_N$(100k)			100kHz Offset from Carrier		-130	-127.4	dBc/Hz
$Φ_N$(1M)			1MHz Offset from Carrier		-141	-138	dBc/Hz
$Φ_N$(10M)			10MHz Offset from Carrier and Noise Floor		-153	-150	dBc/Hz
$Φ_N$(1k)	Single-side Band Phase Noise 125MHz Output Frequency		1kHz Offset from Carrier		-124	-116	dBc/Hz
$Φ_N$(10k)			10kHz Offset from Carrier		-129	-124.9	dBc/Hz
$Φ_N$(100k)			100kHz Offset from Carrier		-128	-125.4	dBc/Hz
$Φ_N$(1M)			1MHz Offset from Carrier		-139	-137	dBc/Hz
$Φ_N$(10M)			10MHz Offset from Carrier and Noise Floor		-151	-150	dBc/Hz
t_{jit}(per)	Period Jitter, Peak-to-Peak	QA[0:3]	f_{OUT} = 125MHz		3.0	8.1	ps
		QB[0:1]	f_{OUT} = 100MHz		3.2	7.4	ps
		QC	f_{OUT} = 50MHz, V_{DDOC} = 3.3V		6	28	ps
			f_{OUT} = 50MHz, V_{DDOC} = 2.5V		7	33	ps
			f_{OUT} = 50MHz, V_{DDOC} = 1.8V		11	39	ps
		QREF[0:2]	f_{OUT} = 25MHz		2.4	4.0	ps

Table 7. AC Characteristics, (Continued)

V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, V_{DDORn},[1] V_{DDOC} = (2.5V to 3.3V) ±5%, 1.8V ± 0.2V, T_A = -55°C to 105°C[2, 3]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$t_{jit(cc)}$	Cycle-to-Cycle Jitter	QA[0:3]	f_{OUT} = 125MHz		9	16	ps
		QB[0:1]	f_{OUT} = 100MHz		11	20	ps
		QC	f_{OUT} = 50MHz, V_{DDOC} = 3.3V		12	27	ps
			f_{OUT} = 50MHz, V_{DDOC} = 2.5V		13	41	ps
			f_{OUT} = 50MHz, V_{DDOC} = 1.8V		44	113	ps
		QREF[0:2]	f_{OUT} = 25MHz		19	33	ps
tsk(b)	Bank Skew[4, 5]	QA[0:3]				25	ps
		QB[0:1]				30	ps
		QREF[0:2]				65	ps
t_R / t_F	Output Rise/Fall Time	Differential Outputs	20% to 80%		150	250	ps
		Single-ended Outputs	20% to 80%		375	750	ps
t_{LOCK}	PLL Lock Time				73		ms
odc	Output Duty Cycle	QA[0:3]	f_{OUT} = 125MHz	48	50	52	%
		QB[0:1]	f_{OUT} = 100MHz	48	50	52	%
		QC	f_{OUT} = 50MHz	48	50	52	%

NOTE 1. V_{DDORn} denotes V_{DDOR0}, V_{DDOR1}, V_{DDOR2}.

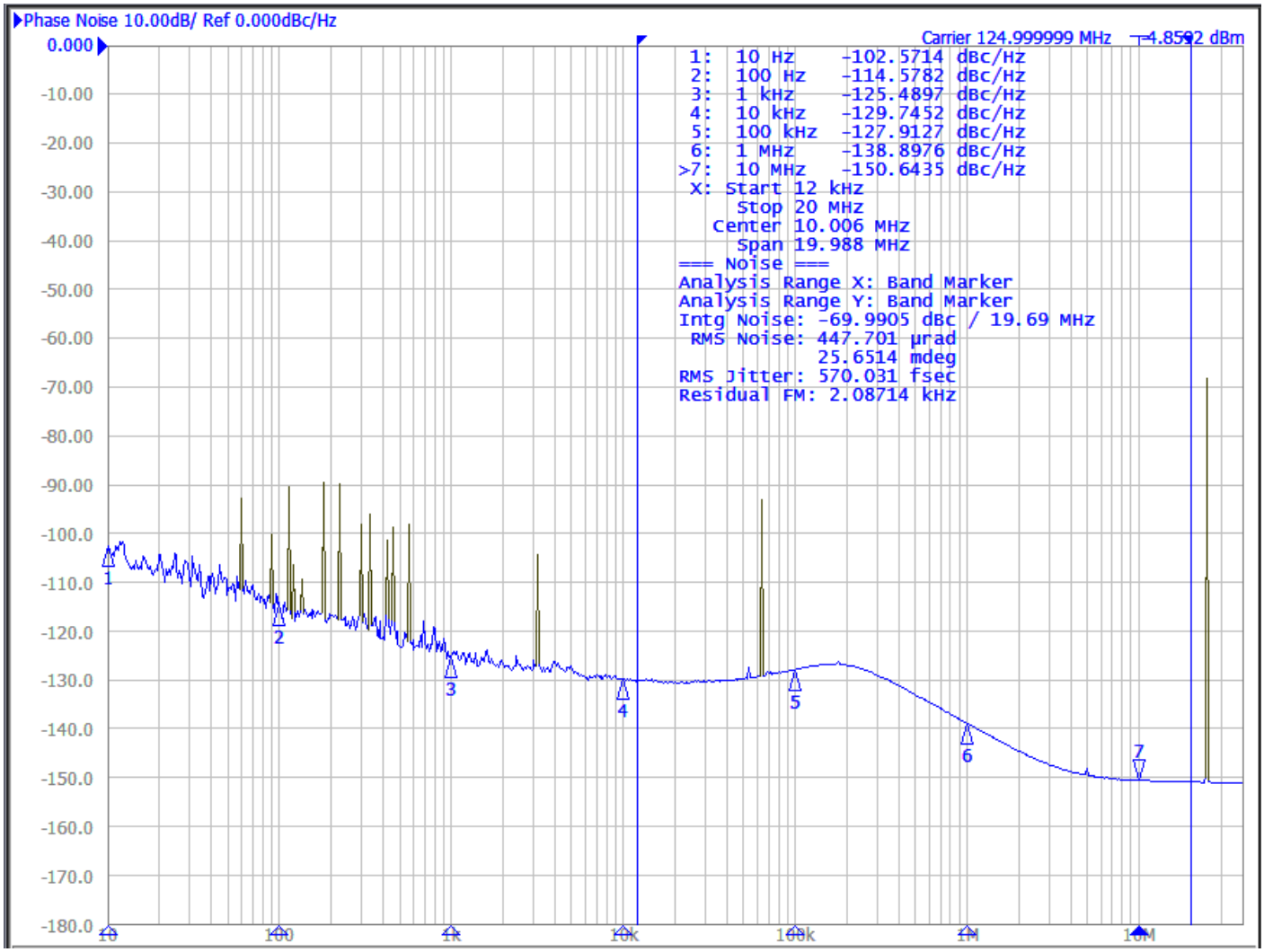
NOTE 2. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 3. f_{REF} = 25MHz.

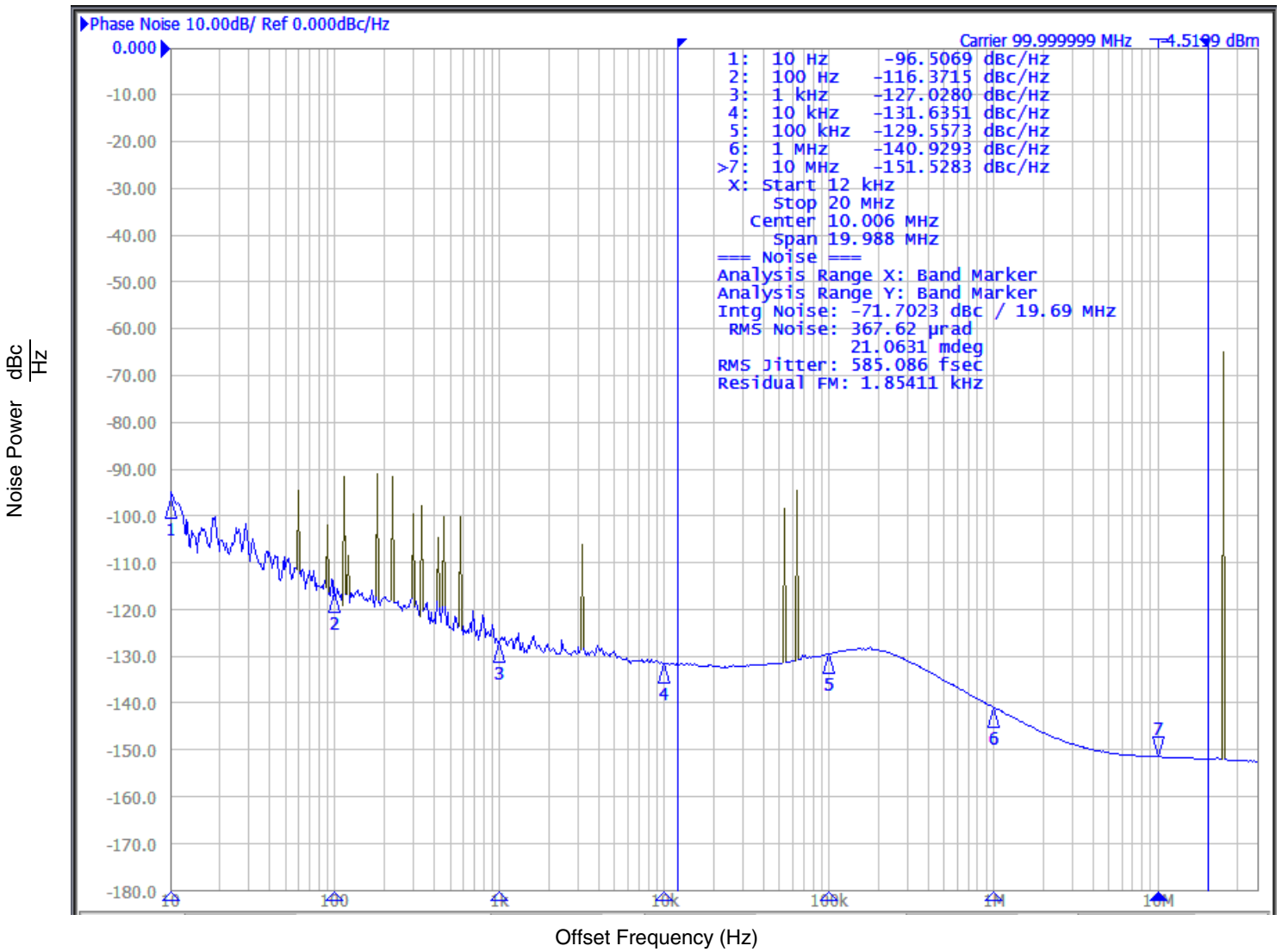
NOTE 4. Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

NOTE 5. This parameter is defined in accordance with JEDEC Standard 65.

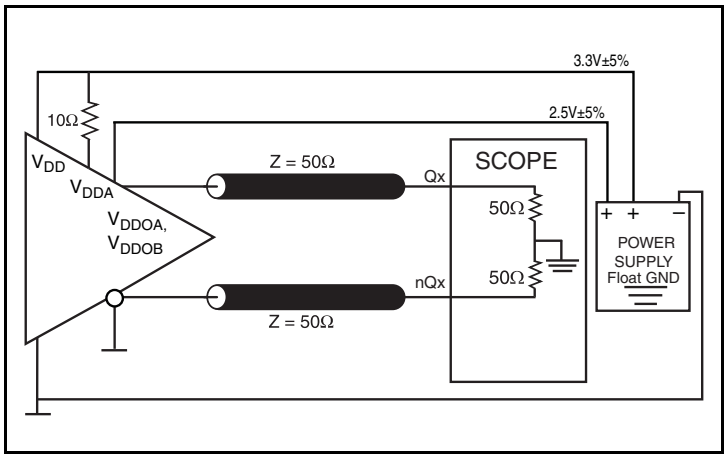
Typical Phase Noise at 125MHz, 2.5V (QA Outputs)



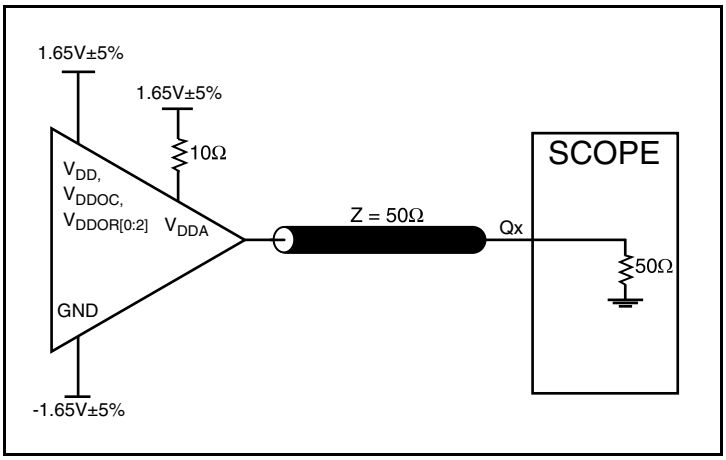
Typical Phase Noise at 100MHz, 2.5V (QB Outputs)



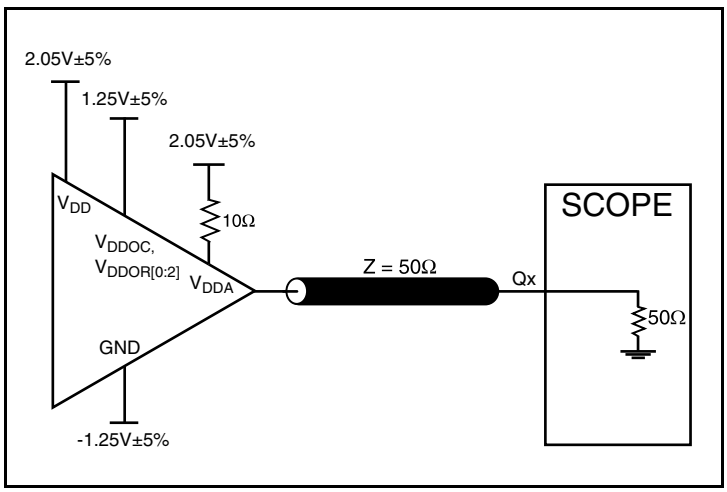
Parameter Measurement Information



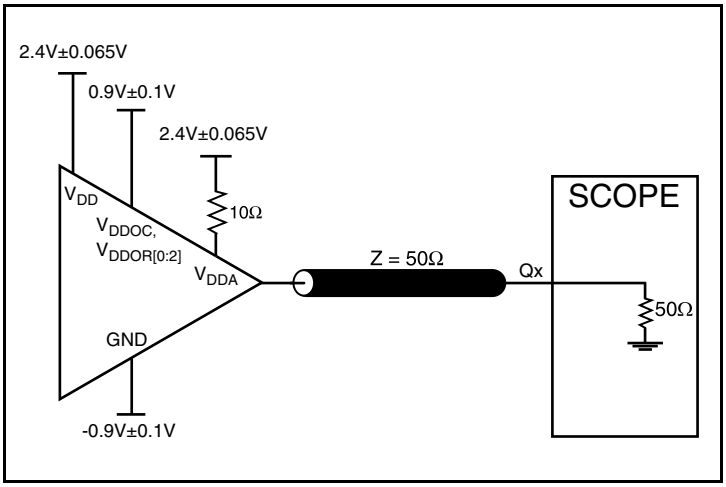
LVDS 3.3V Core/2.5V Output Load AC Test Circuit



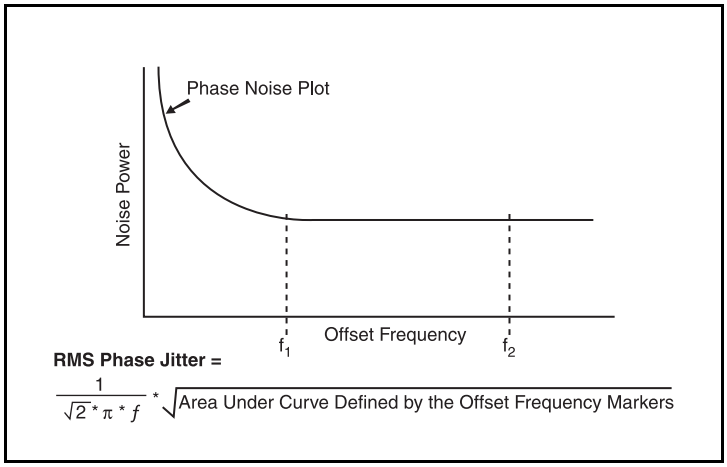
LVCMOS 3.3V Core/3.3V Output Load AC Test Circuit



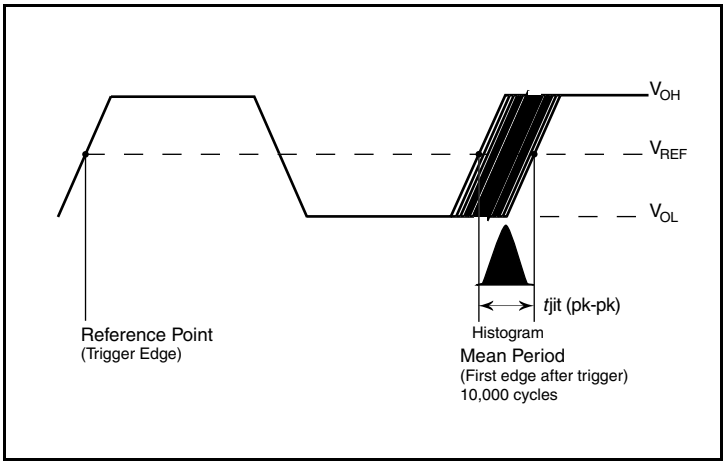
LVCMOS 3.3V Core/2.5V Output Load AC Test Circuit



LVCMOS 3.3V Core/1.8V Output Load AC Test Circuit

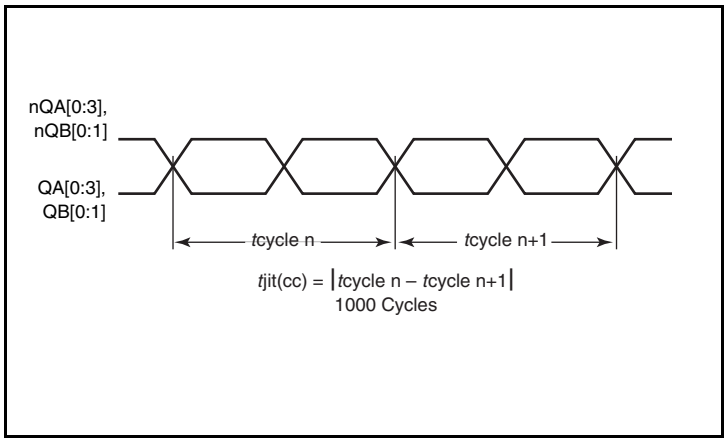


RMS Phase Jitter

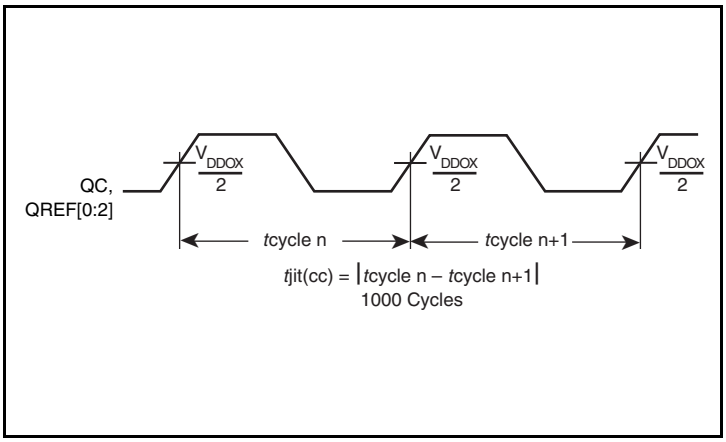


Period Jitter

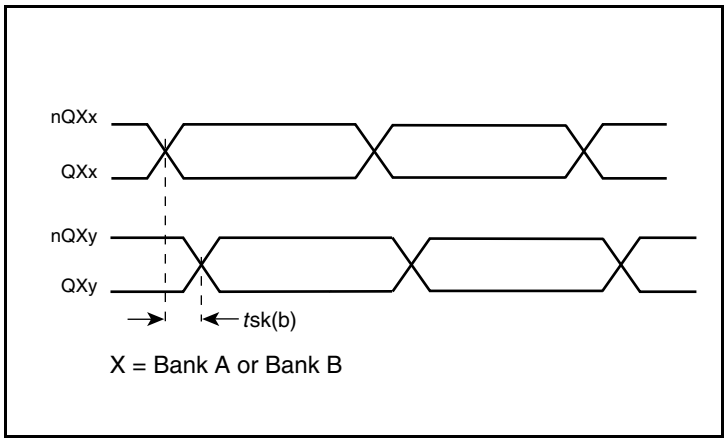
Parameter Measurement Information, continued



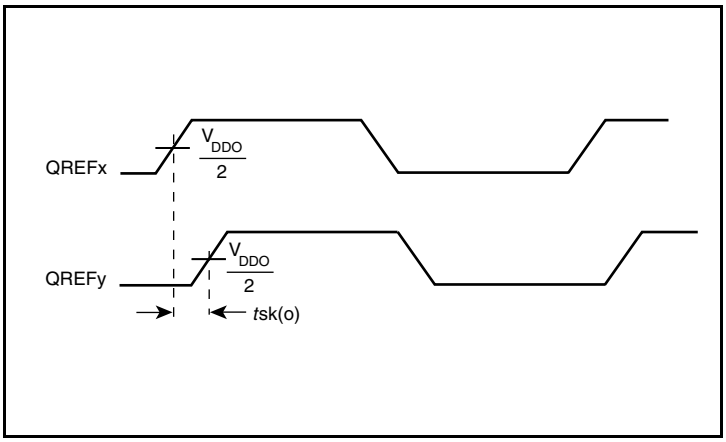
LVDS Cycle-to-Cycle Jitter



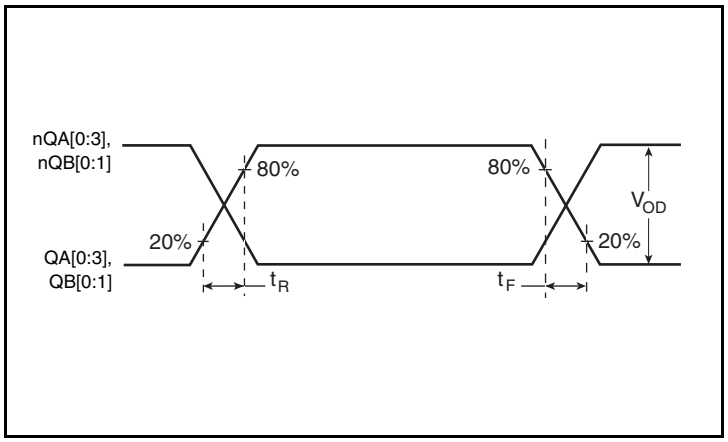
LVCMOS Cycle-to-Cycle Jitter



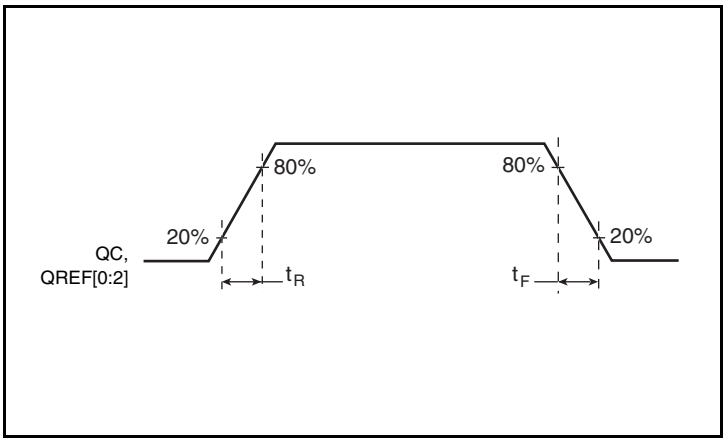
LVDS Bank Skew



LVCMOS Bank Skew

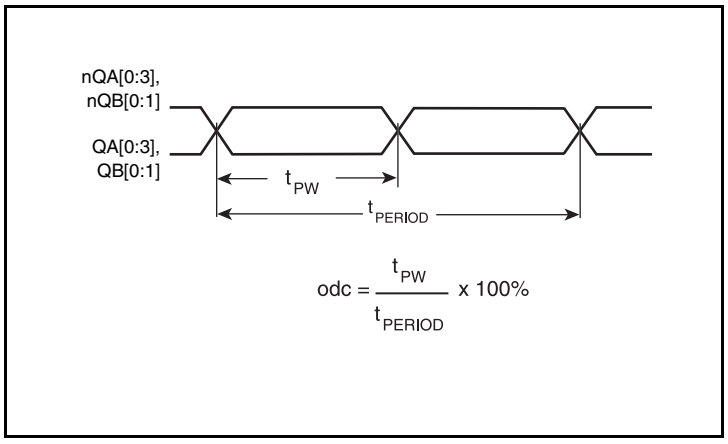


LVDS Output Rise/Fall Time

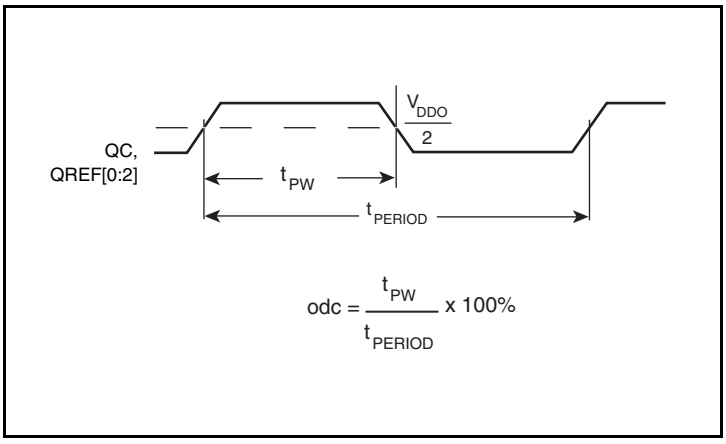


LVCMOS Output Rise/Fall Time

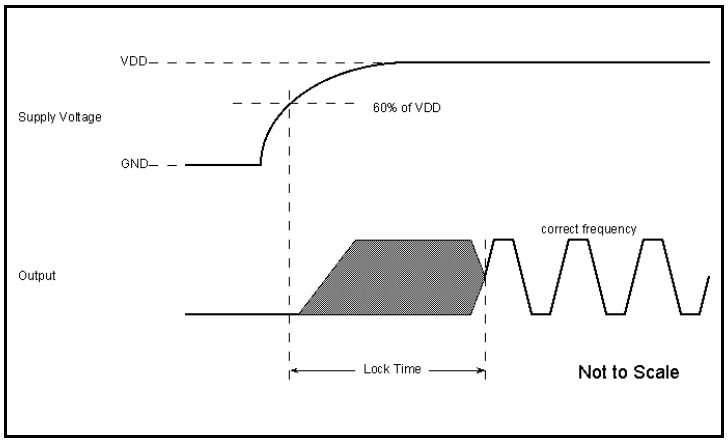
Parameter Measurement Information, continued



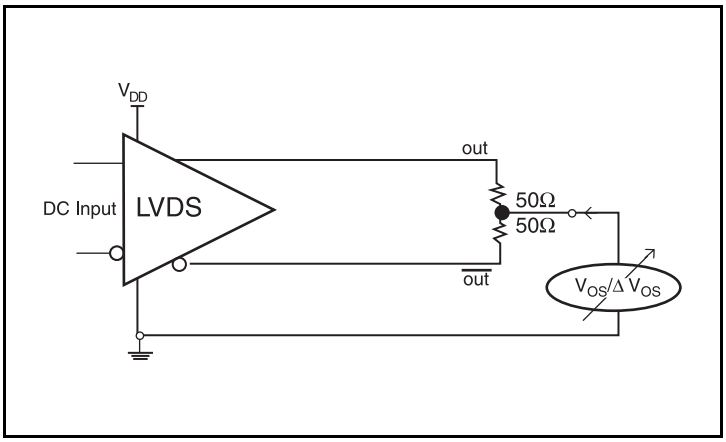
LVDS Output Duty Cycle/Pulse Width/Period



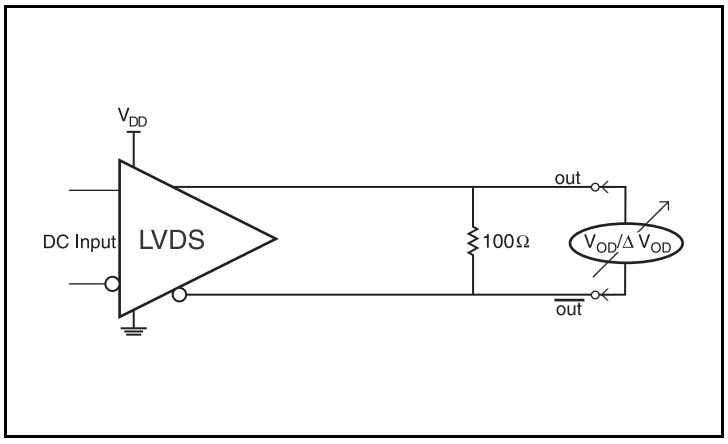
LVCMOS Output Duty Cycle/Pulse Width/Period



PLL Lock Time



Offset Voltage Setup



Differential Offset Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pull-down resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating We recommend that there is no trace attached.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT output can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 1A shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 1B shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

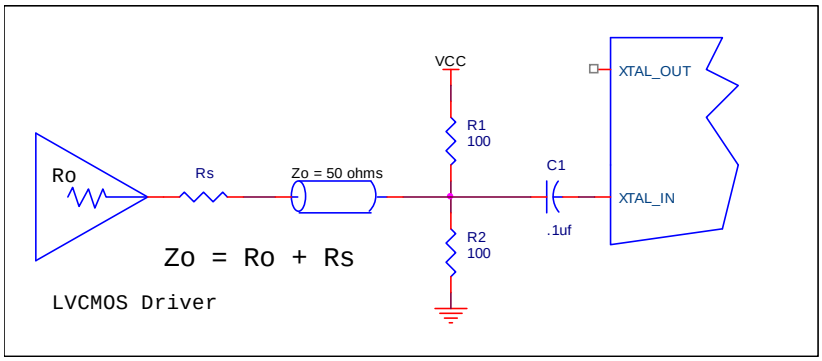


Figure 1A. Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

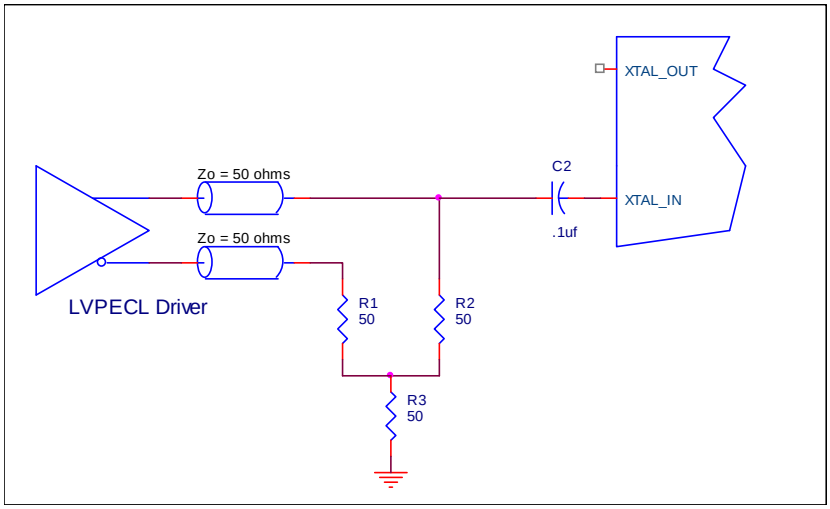


Figure 1B. Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

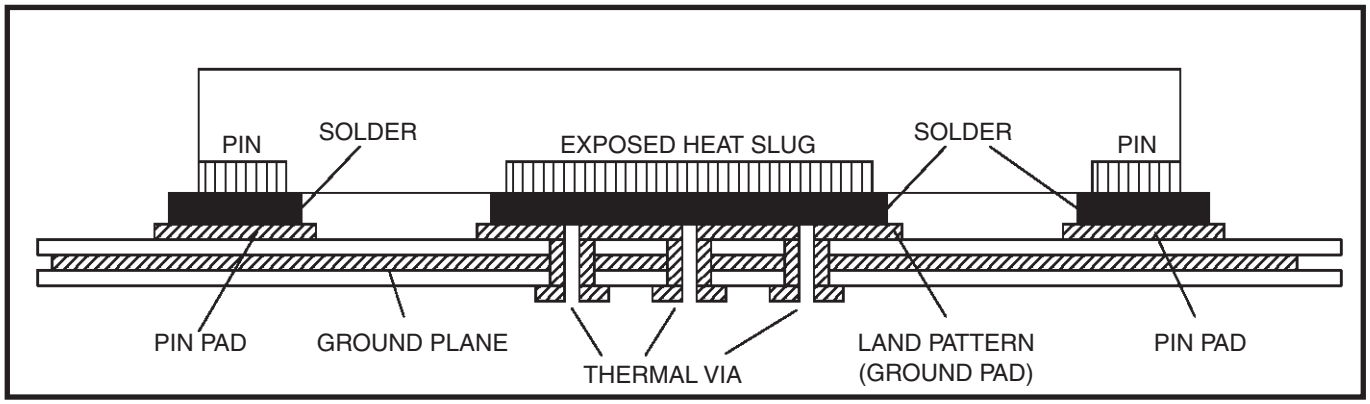


Figure 2. Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

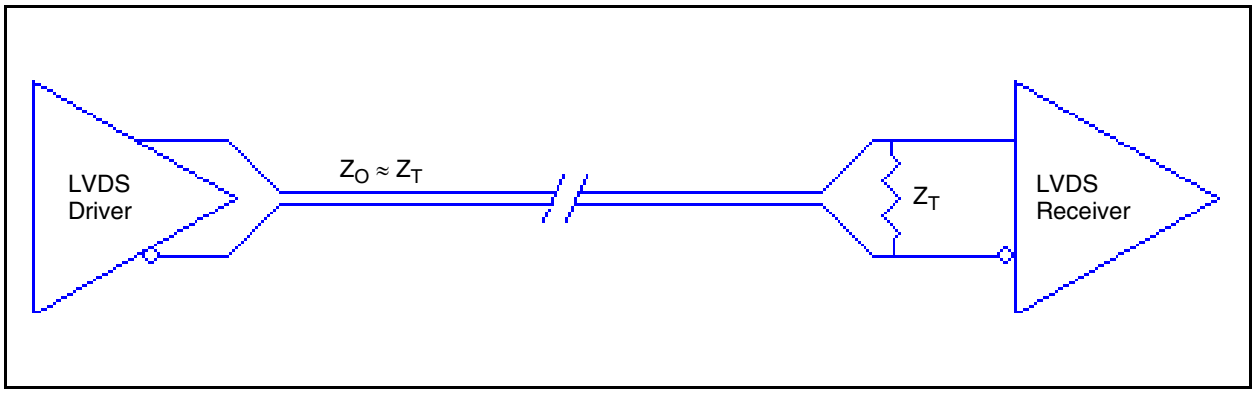


Figure 3A. Standard LVDS Termination

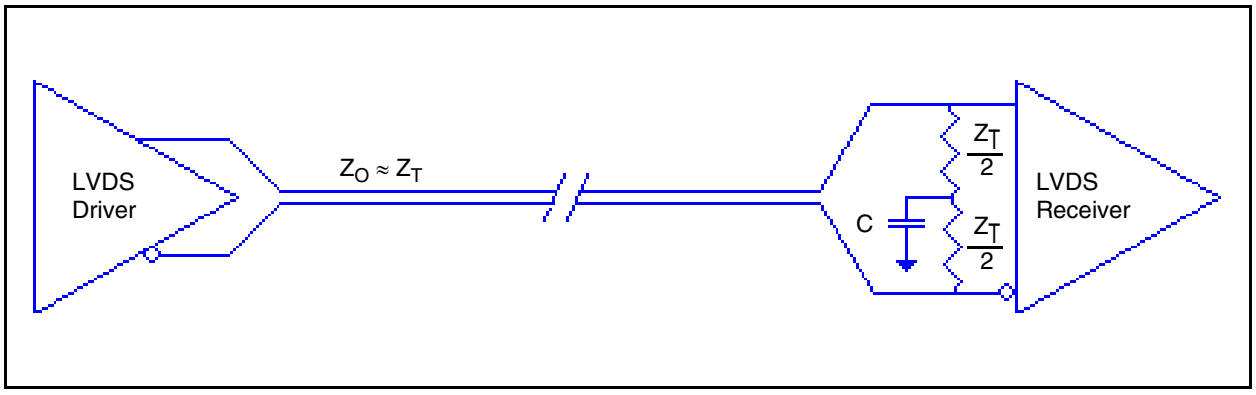


Figure 3B. Optional LVDS Termination

Schematic Layout

Figure 4 (next page) shows an example 8V44S269 application schematic in which the device is operated at $V_{DD} = V_{DDOR0} = V_{DDOR1} = V_{DDOR2} = 3.3V$ and $V_{DDOA} = V_{DDOB} = 2.5V$.

This example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

Two different differential terminations are depicted. QA0 is the standard LVDS termination. QA3 is an example demonstrating how the IDT LVDS outputs can be directly AC coupled to IDT CLK, nCLK clock receiver inputs where the internal bias resistors of the receiver guarantee that the AC coupled LVDS clock is within the common mode range of the receiver.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V44S269 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL. The Murata BLM18BB221SN1B ferrite bead shown in the schematic was selected for the flat frequency response realized with the associated filter capacitors. The rated current for this bead is 450mA which will accommodate the maximum current for each power filter.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 10 ohm V_{CCA} resistor and the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull-up and pull-down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

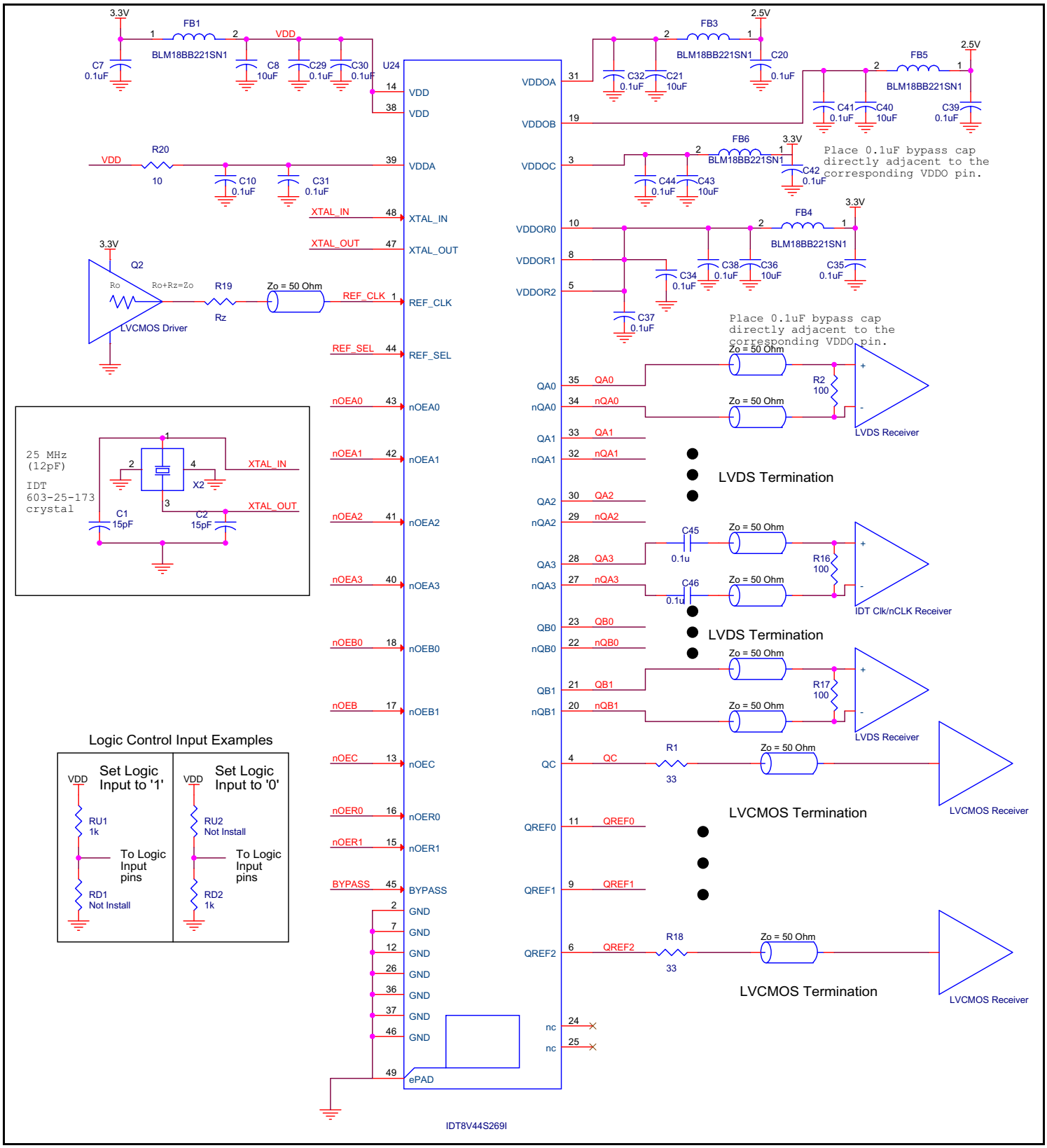


Figure 4. 8V44S269 Application Schematic

Power Considerations

The 8V44S269 device was designed and characterized to operate within the ambient extended temperature range of -55°C to 105°C. The ambient temperature represents the temperature around the device, not the junction temperature. Extreme care must be taken to avoid exceeding the 125°C junction temperature, potentially damaging the device.

Equations and example calculations are also provided below.

1. Power Dissipation.

The power dissipation for the 8V44S269 is the product of supply voltage and total I_{DD}.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V at ambient temperature of 105°C, QREFn = 25MHz, QC = 50MHz, QAn = 125MHz, QBn = 100MHz.

I_{DD_MAX} = 91mA

I_{DDA_MAX} = 16mA

$I_{DDOA\_MAX} + I_{DD0B\_MAX} + I_{DDOC\_MAX} + I_{DDORn\_MAX}$ = 141mA

- Power(core)$_{\_max}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (91mA + 16mA) = **370.76mW**
- LVDS and LVCMOS Outputs Power(output)$_{\_max}$ = 3.465V * 141mA = **488.57mW**
- Total Power$_{_max}$ (3.465V, with all outputs switching) = 370.76mW + 488.57mW = **859.33mW**

2. Junction Temperature.

Junction temperature, Tj, signifies the hottest point on the device and exceeding the specified limit could cause device reliability issues. The maximum recommended junction temperature is 125°C.

For devices like this and in systems where most heat escapes from the bottom exposed pad of the package, θ_{JB} is the primary thermal resistance of interest.

The equation to calculate Tj using θ_{JB} is: $Tj = \theta_{JB} * P_D + T_B$

Tj = Junction Temperature

θ_{JB} = Junction-to-Board Thermal Resistance

P_D = Device Power Dissipation (example calculation is in section 1 above)

T_B = Board Temperature

In order to calculate junction temperature, the appropriate junction-to-board thermal resistance θ_{JB} must be used. Assuming a 2-ground plane board, the appropriate value of θ_{JB} is 1.93°C/W per Table 8 below.

Therefore, Tj for a PCB maintained at 115°C with the outputs switching is:

115°C + 0.859W * 1.93°C/W = 116.7°C which is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, heat transfer method, the type of board (multi-layer) and the actual maintained board temperature. The below table is for two ground planes. The thermal resistance will change as the number of layers in the board changes or if the board size change and other changes in other factors impacts heat dissipation in the system.

Table 8. Thermal Resistances for a 48-Lead VFQFN Package[1, 2, 3]

Meters per Second	0	1	2
Theta J_B	1.93°C/W	1.93°C/W	1.93°C/W
Theta J_A	26.11°C/W	22.53°C/W	21.04°C/W
Theta J_C	18.8°C/W	18.8°C/W	18.8°C/W

NOTE 1. Applicable to PCBs with two ground planes.

NOTE 2. ePAD size is 5.65mm x 5.65mm and connected to ground plane in PCB through 5 x5 Thermal Via Array.

NOTE 3. In devices where most of the heat exits through the bottom ePAD, θ_{JB} is commonly used for thermal calculations.

Reliability Information

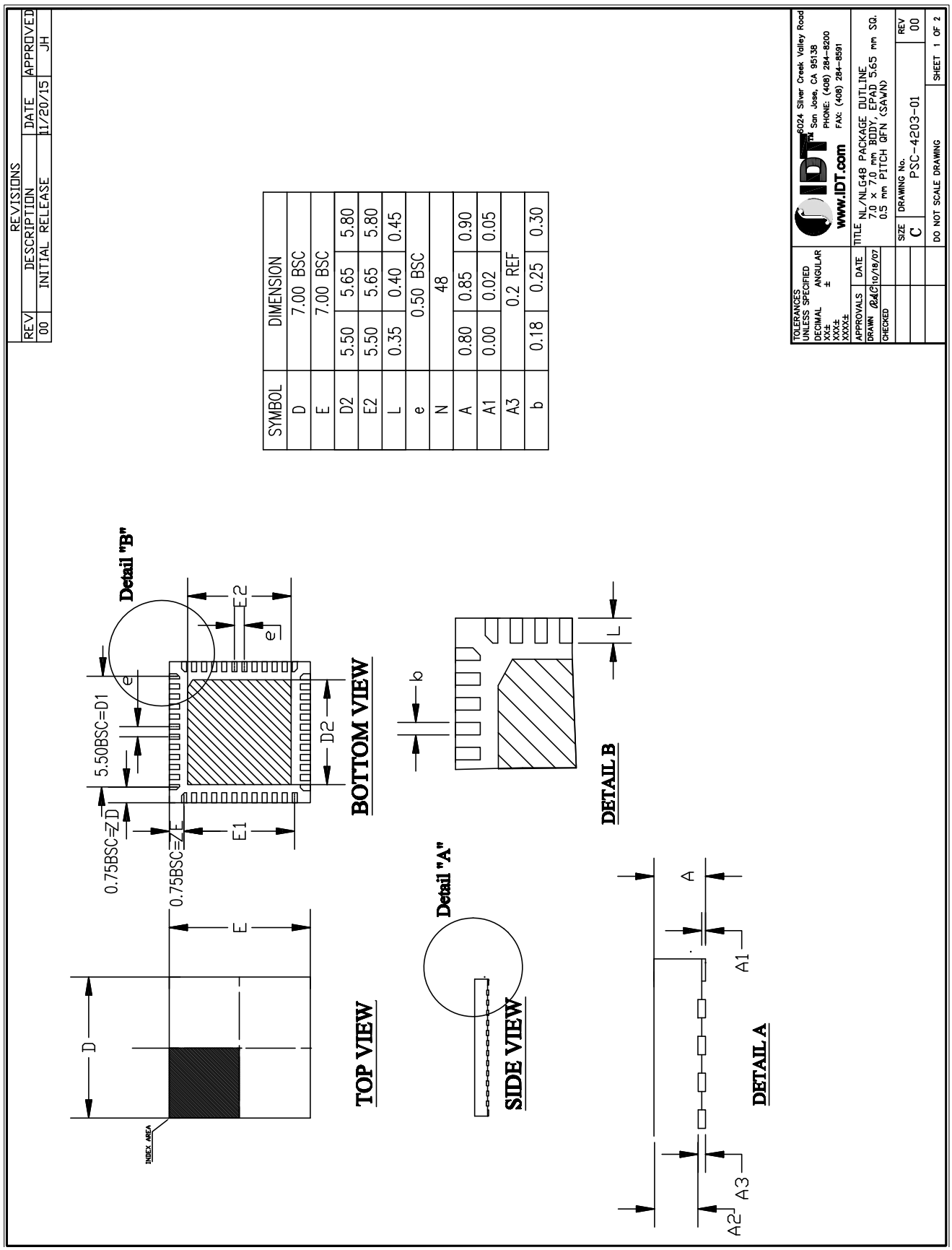
Table 9. Thermal Resistances for a 48 Lead VFQFN Package

Meters per Second	0	1	2
Theta J_B	1.93°C/W	1.93°C/W	1.93°C/W
Theta J_A	26.11°C/W	22.53°C/W	21.04°C/W
Theta J_C	18.8°C/W	18.8°C/W	18.8°C/W

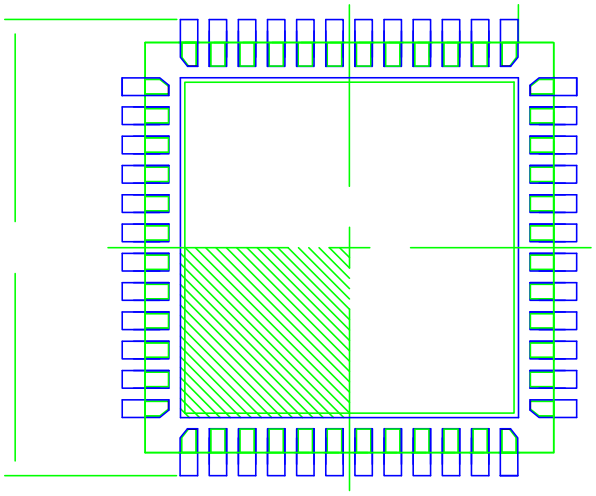
Transistor Count

8V44S269 transistor count: 11,242

48 Lead VFQFN Package Information



48 Lead VFQFN Package Information



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN BLACK.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V44S269NLGI	IDT8V44S269NLGI	48 Lead VFQFN, Lead-Free	Tray	-55°C to 105°C
8V44S269NLGI8	IDT8V44S269NLGI	48 Lead VFQFN, Lead-Free	Tape & Reel	-55°C to 105°C

Revision History Sheet

Table	Page	Description of Change	Date
	1	Corrected datasheet title head.	5/9/2016

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