P9412

30W Wireless Transmitter/Receiver (TRx)

The P9412 is a 30W highly integrated single-chip wireless power Wattshare™ transmitter/receiver IC (TRx) with a high-performance capacitive divider. The device can be configured to receive or transmit AC power through magnetic induction. When the device is configured as a wireless power transmitter (Tx), it uses on-chip full/half-bridge inverter, PWM generator, modulator/demodulator (for communication) and micro controller to produce an AC power signal to drive external L-C tank. As a wireless power receiver (Rx), the device receives AC power from a wireless transmitter and converts it to a rectified output voltage, which can be used to power downstream devices or supply the charger input in mobile applications.

The P9412 integrates a high-efficiency synchronous full bridge rectifier and control circuitry to modulate the load and send message packets to the Transmitter for optimized power delivery. The device features Multiple-Time Programmable (MTP) non-volatile memory which allows easy firmware updates.

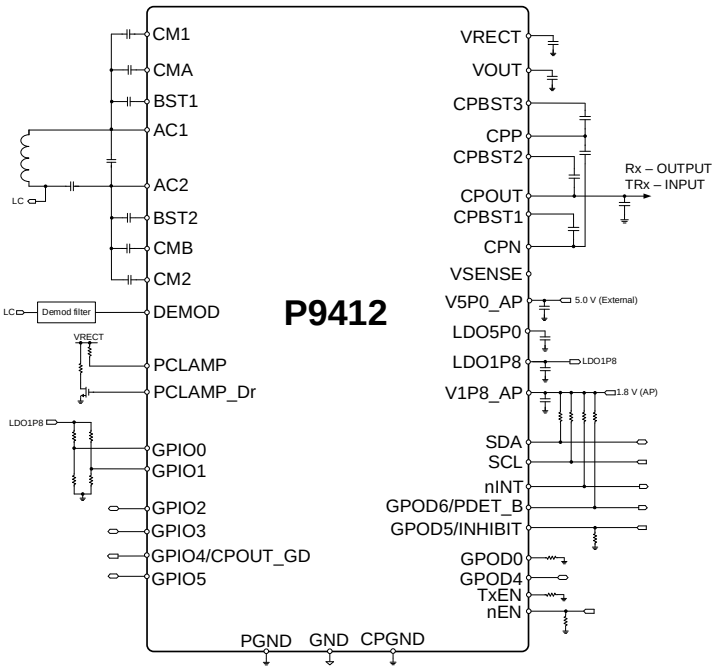
The P9412 includes over-current, over-voltage, and over-temperature protections. Fault conditions are managed by an industry-leading 32-bit ARM® Cortex®-M0 processor offering high programmability with low standby power ideal for mobile applications. The processor can also control GPIOs to indicate operating and fault modes. The device is available in a WLCSP-81 package.

Applications

- Smart phone
- Other mobile applications

Features

- Single-chip Magnetic Induction Wireless Power Transmitter/Receiver
- WPC 1.3 compatible
- Supports proprietary modes
- Delivers up to 30W as a receiver
- Delivers over 6W as a transmitter
- Integrated high-performance synchronous rectifier, LDO, and capacitor divider
- Reliable over-voltage clamping
- Best-in-class EMI performance (in Bypass mode)
- Proprietary Rx-to-Tx modulation/demodulation for two-way communication
- Tx-to-Rx (Backchannel) communication
- 24kB MTP non-volatile memory for expanded feature support
- Embedded 32-bit ARM® Cortex®-M0 processor
- Supports I²C 400kHz standard interface and GPIOs
- 0.4mm pitch WLCSP-81 4.02 × 4.01 mm package



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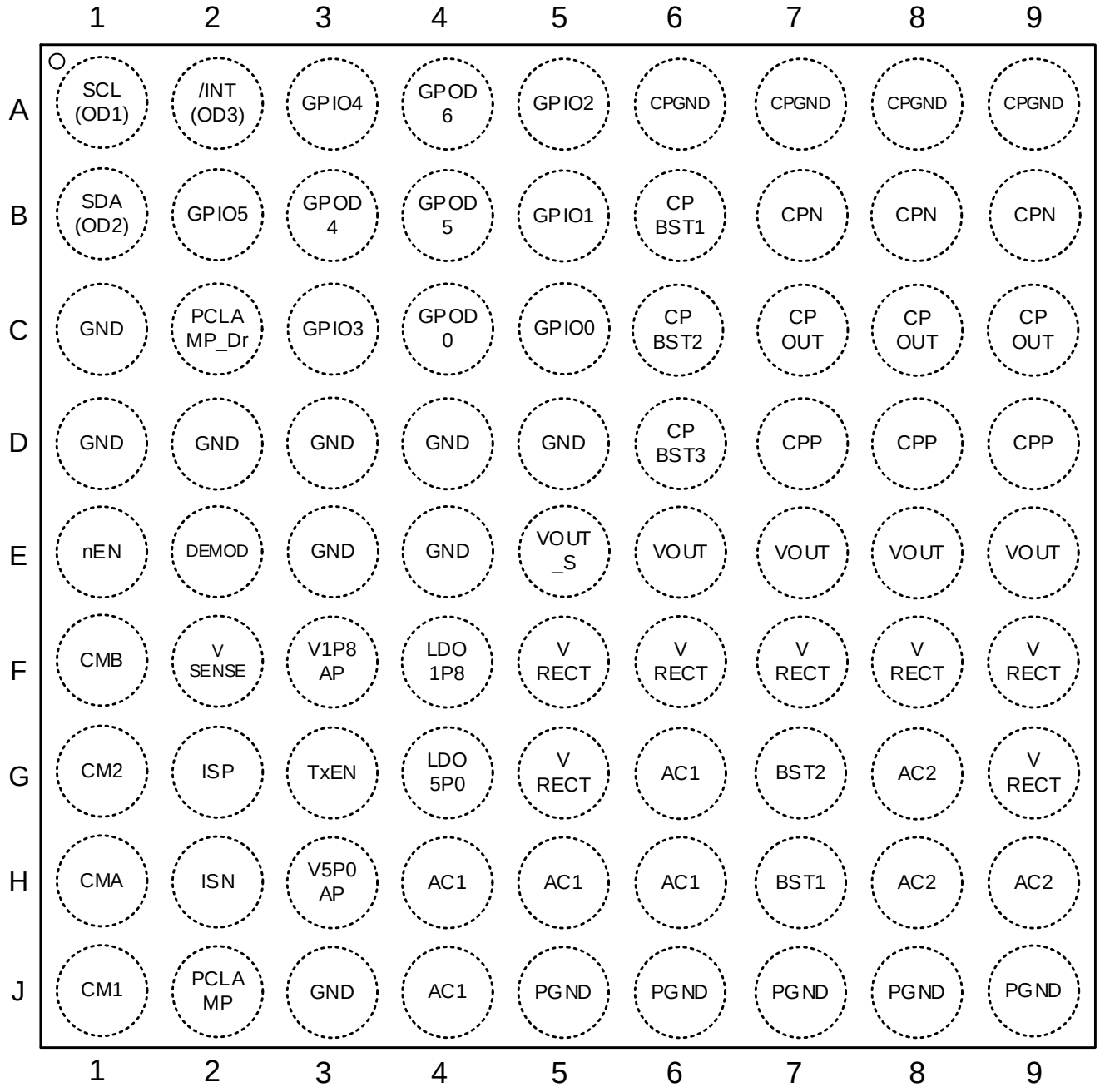

Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
A1	SCL (OD1)	I/O	Clock for I2C Serial Interface with AP (SCL). Connect a pull-up resistor to the system I/O supply.
A2	nINT (OD3)	O	Open-drain GPIO; active-LOW interrupt from the P9412 to the AP. Connect an external pull-up to V1P8_AP with a 10kΩ - 100kΩ resistor. Output is active-LOW when status change occurs in the interrupt registers.
A3	GPIO4	I/O	General purpose push-pull I/O, referenced to LDO1P8. May be left floating if unused.
A4	GPOD6	O	Ping Detect (PDET) output indicator and can be left floating if unused.
A5	GPIO2	I/O	General purpose push-pull I/O, referenced to LDO1P8. May be left floating if unused.
A6, A7, A8, A9	CPGND	GND	Ground for capacitor divider. All CPGND pins must be connected together with PGND and GND externally.
B1	SDA (OD2)	I/O	Data for I2C Serial Interface with AP (SDA). Connect a pull-up resistor to the system I/O supply.
B2	GPIO5	I/O	General purpose push-pull I/O, referenced to LDO1P8. It can be left floating if unused.
B3	GPOD4	I/O	General Purpose Open Drain I/O. Default state is configured as CPOUT_GD function. It can be left floating if unused.
B4	GPOD5	I	Active High SW Inhibit input. When active the device will not connect wirelessly. Connect to GND if unused.
B5	GPIO1	I	Reported Q-factor ADC input for EPP Rx mode. Connect to a resistor divider from LDO1P8 and GND. Connect to GND if unused.
B6	CPBST1	O	Bootstrap capacitor connection to a CPN. Powers driver for NFET associated with CPN and CPOUT.
B7, B8, B9	CPN	I/O	Capacitor Divider flying capacitor negative connection. Place two or three 22µF capacitors between CPP and CPN pin.
C1, D1, D2, D3, D4, D5, E3, E4, J3	GND	GND	Ground. All GND pins must be connected together with PGND and CPGND externally.
C2	PCLAMP_Dr	O	Output gate driver pin for External Clamping Circuit (5V IO level). May be left floating if unused (only applicable for <15W designs). Connect as shown in reference design for >15W designs.
C3	GPIO3	I/O	General purpose push-pull I/O, referenced to LDO1P8. May be left floating if unused.
C4	GPOD0	I	Active low PDET enable input. Connect to GND if not used.
C5	GPIO0	I	Reported Q-factor ADC input for EPP Rx mode. Connect to a resistor divider from LDO1P8 and GND. Connect to GND if unused (forces device to use register value to report Q in EPP Rx mode).
C6	CPBST2	O	Bootstrap capacitor connection to CPout. Powers driver for NFET associated with CPOUT and CPP.
C7, C8, C9	CPOUT	I/O	Output of capacitor divider converter or MDLO in Bypass Configuration in Rx mode or input for TRx mode. Connect to load switch and then to system load/TRx power supply and two 22µF ceramic capacitors to GND.
D6	CPBST3	O	Bootstrap capacitor connection to CPP. Powers driver for NFET associated with CPP and CPout.
D7, D8, D9	CPP	I/O	Capacitor Divider flying capacitor positive connection. Place two or three 22µF capacitors between CPP and CPN pin.
E1	nEN	I	Active-low enable pin. When it is pulled-up High by the AP GPIO, the rectifier will be set in Diode mode, internal regulator do not activate, and firmware does not load. While it is pulled-down Low, the device operates as programmed by firmware.
E2	DEMOD	I	Tx mode Communication Demodulator input. Connect to LC node via diode and DEMOD filter.
E5	VOUT_S	O	Main LDO output voltage sensing pin. Connect close to VOUT bypass capacitor with separate connection from the MLDO VOUT output connection (pins E6-E9).

Number	Name	Type	Description
E6, E7, E8, E9	VOUT	O	Main LDO output pin. Connect 3 × 10μF or more capacitors to ground.
F1	CMB	O	High-voltage open-drain modulation FET. Connect a capacitor from AC2 to CMB.
F2	VSENSE	I	Voltage sensing. Connect to sensing point as close as possible. Do not apply more than 5V during operation.
F3	V1P8AP	I	Application processor (AP) power input. The V1P8AP pin should be connected directly to the PMIC voltage rail. This pin must be powered to enable PDET function.
F4	LDO1P8	O	1.8V LDO for providing Internal power and ARM-M0 processor. Connect to a capacitor to GND.
F5, F6, F7, F8, F9, G5, G9	VRECT	O	Filter capacitor connection for the synchronous rectifier output. Connect to capacitors to GND.
G1	CM2	O	High-voltage open-drain modulation FET. Connect a capacitor from AC2 to CM2.
G2	ISP	I	Reverse external current sensing positive input. Connect to CPout if not used.
G3	TxEN	I	Tx mode active-high enable pin. Overrides /EN input pin if used. Connect to GND if not used.
G4	LDO5P0	O	Internal 5V LDO for chip power only. Connect to a capacitor to GND.
G6, H4, H5, H6, J4	AC1	I/O	AC1 power input. Connect to RX LC tank (due to symmetry may connect to Rx coil or Resonance Capacitor).
G7	BST2	O	Bootstrap capacitor for driving the high side N-MOSFET of the internal rectifier. Connect to a capacitor from AC2 to BST2.
G8, H8, H9	AC2	I/O	AC2 power input. Connect to RX LC tank (due to symmetry may connect to Rx coil or Resonance Capacitor).
H1	CMA	O	High-voltage open-drain modulation FET. Connect a capacitor from AC1 to CMA.
H2	ISN	I	Reverse current sensing negative input. Connect to CPout if not used.
H3	V5P0_AP	I	Application processor (AP) power input. The V5P0_AP pin can be directly connected to 5V external power to replace LDO5P0 voltage to reduce device power consumption for high voltage operation. Leave it floating if not used.
H7	BST1	O	Bootstrap capacitor for driving high side N-MOSFET of the internal rectifier. Connect a capacitor from AC1 to BST1.
J1	CM1	O	High-voltage open-drain modulation FET. Connect a capacitor from AC1 to CM1.
J2	PCLAMP	I	High-voltage open-drain input for linear clamping during OVP events. Connect a resistor from this pin to VRECT for > 5W operation. Short directly to VRECT for 5W or lower power applications.
J5, J6, J7, J8, J9	PGND	GND	Power Ground. All PGND pins must be connected together with GND and CPGND externally.

2. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the P9412 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol/Pins	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction temperature	-	-	150	°C
T_S	Storage temperature	-	-55	150	°C
HBM – All Pins except AC1,AC2,Vrect	ESD – Human Body Model	-	-	2000	V
HBM - AC1,AC2,Vrect	ESD – Human Body Model	-	-	1000	V
CDM	ESD – Charged Device Model	-	-	500	V
AC1, AC2, CM1, CM2, CMA, CMB, VRECT, PCLAMP	Maximum Voltage		-0.3	26.5	V
LDO1P8, V1P8AP, GPIO0 – GPIO5	Maximum Voltage		-0.3	2	V
DEMOD, LDO5P0, V5P0AP, nEN, GPOD0, SCL (OD1), SDA (OD2), /INT (OD3), GPOD4-GPOD6, PLCAMP_Dr, VENSE, TxEN	Maximum Voltage		-0.3	6	V
BST1, BST2	Maximum Voltage		-0.3	AC1+5, AC2+5	V
CPOUT, CPN, CPP, ISP, ISN	Maximum Voltage		-0.3	13	V
CPBST1	Maximum Voltage		-0.3	CPN + 5	V
CPBST2	Maximum Voltage		-0.3	CPOUT + 5	V
CPBST3	Maximum Voltage		-0.3	CPP + 5	V
CPGND, GND, PGND	Maximum Voltage		-0.3	0.3	V
VOUT, VOUT_S	Maximum Voltage		-0.3	21.5	V
CPOUT Output Current	Maximum RMS Current			3.3	A
AC1, AC2	Maximum RMS Current1			2	A
VOUT Output Current	Maximum RMS Current			1.65	A

3. Thermal Characteristics [2,3,4,5]

Table 3. Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}[4]	Theta JA. Junction to ambient.	25.5	°C/W
θ_{JB}[4]	Theta JB. Junction to board.	1.5	°C/W
θ_{JC}[4]	Theta JC. Junction to case.	0.08	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)	MSL 1	-

1. Rectifier Mosfets are fully turned on.
2. The maximum power dissipation is PD(MAX) = (TJ(MAX) - TA) / θJA where TJ(MAX) is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
3. This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" × 4.5" in still air conditions.
4. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.
5. For the WLCSP (AHG81) package, connecting PGND balls and at least TBD# other CSP balls (TBD# thermal balls total) to internal/external ground planes from top to bottom sides of the PCB is recommended for improving the overall thermal performance.

4. Electrical Characteristics

V_{RECT} = 5.5V, C_{LDO1P8}=C_{LDO5P0}=1.0µF, C_{VRECT}=3×10µF, C_{VOUT}=3×10µF, C_{CPOUT}=3×22µF, unless otherwise noted, T_A = -5°C to 85°C, Typical values are at T_A = 25°C.

Table 4. Electrical Characteristics

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
Quiescent Current						
$I_{RECT-ACTIVE}$	I_{RECT} active current	No external load on VRECT, LDO5P0, LDO1P8, rectifier not switching, nEN=Low		6	10	mA
$I_{RECT-DIS}$	I_{RECT} Disable current	No external load on VRECT, LDO5P0, LDO1P8, rectifier not switching, nEN=High		1		mA
Thermal Protection						
T_{SD}	Thermal Shutdown	Rising to shut down the device		140		°C
		Threshold falling to resume		130		°C
Synchronous Rectifier						
$R_{DSON\_RECT\_FET}$[NOTE2]	Full bridge MOSFET			50		mΩ
$V_{IN\_VRECT\_Rx}$[NOTE3]	VRECT input operating voltage range in Rx mode		3.5		21.5	V
$V_{IN\_UVLO\_RISING\_Rx}$	UVLO threshold in rising	VRECT rising with no load		2.55		V
$V_{UVLO\_HYS\_Rx}$	UVLO hysteresis	VRECT falling (main LDO shutdown)		200		mV
Over Voltage Protection on V_{RECT}						
V_{OVP_VRECT}	OVP threshold	Rising on VRECT	22	24	26	V
$V_{OVP\_VRECT\_HYS}$	OVP Hysteresis			1.5		V
$V_{PRE\_CLAMP\_TH}$	Pre-clamp protection enabled threshold	V_{OVP_VRECT} percentage of voltage to trigger PCLAMP		90		%
$\%I_{PCLAMP}$	Pclamp current accuracy	VRECT=20V, set at 63mA		±10		%

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
PCLAMP_DR						
V_{OH}	Output High Voltage	IOH=4mA	4.0	4.3		V
V_{OL}	Output Low Voltage	IOL=8mA		0.3	0.6	V
Analog-to-Digital Converter (ADC)						
N	Resolution			12		bit
V_{IN_FS}	Full Scale input voltage			2.1		V
f_{SAMPLE}	Sample Frequency			67.5		kSa/s
Channel	Number of Channels			16		#
Enable (nEN)						
V_{IH}	Input High Threshold		1.6			V
V_{IL}	Input Low Threshold				0.25	V
I_{nEN_LKG}	Leakage Current	nEN=0V	-1		1	µA
		nEN=5V		2.5		µA
Clock						
F_{CLOCK}	Clock Frequency			60		MHz
General Purpose I/O (Push-Pull Output Type)						
V_{OH}	Output logic High	I_{OH}=8mA		1.7		V
V_{OL}	Output logic Low	I_{OL}=8mA		0.36		V
V_{IH}	Input High Threshold	V_{RISING}=0 to 1.8V	1.25	1.2		V
V_{IL}	Input Low Threshold	$V_{FALLING}$=1.8V to 0V, GPIO2 - GPIO5		0.6	0.65	V
V_{IL}	Input Low Threshold	$V_{FALLING}$=1.8V to 0V, GPIO0 and GPIO1.		1.1	1.2	V
I_{GPIO_LKG}(NOTE2)	Leakage Current	V_{PIN}=0V and 1.8V	-1		1	µA
General Purpose I/O (Open-Drain Output Type)						
V_{OL}	Output Low Voltage	I_{SINK}=8mA, V_{PULLUP}=1.8V		0.36		V
I_{GPOD_LKG}(NOTE2)	Leakage Current	V_{PULLUP}=1.8V, T_A=25°C	-1		1	µA
LDO5P0						
V_{LDO5P0}	LDO5P0 regulation voltage	VRECT≥5.5V	4.5	4.9	5.4	V
I_{LDP5P0_LIMIT}(NOTE2)	Current Limit			80		mA
V1P8_AP (1.8V input pin)						
V_{1P8_AP}	Input voltage range		1.7		1.9	V
$V_{POK\_1P8\_AP\_RANGE}$	Power OK range	On V1P8_AP in rising to indicate voltage is applied.	1.8			V
$V_{1P8\_AP\_HYSTERESIS}$	V1P8_AP falling threshold	On V1P8_AP in falling		30		mV
$I_{V1P8\_AP\_INUPT\_CURRENT}$	V1P8_AP input current	V_{1P8_AP}=1.8V, P9412 not powered		5		µA
V5P0_AP (5.0V input pin)						
V_{5P0_AP}	Input voltage range		4.7		5.5	V
$V_{POK\_5P0\_AP\_RANGE}$	Power OK range	On V5P0_AP in rising to indicate voltage is applied.	4.95			V
$V_{5P0\_AP\_HYSTERESIS}$	V5P0_AP falling threshold	On V5P0_AP in falling to indicate voltage removed.		200		mV
$I_{V5P0\_AP\_INPUT\_CURRENT}$	V1P8_AP input current	V_{5P0_AP}=5V, P9412 not powered		1		µA

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
Modulation						
$R_{DSON\_MODU\_FET}$ NOTE2	Modulation MOSFET			1		Ω
Main Low-Drop-Out (MLDO) Regulator (VOUT)						
$V_{MLDO\_VOUT\_RNG}$	programmable VOUT voltage range	VRECT ≥ (Preset VOUT + headroom)	3.5		20	V
$R_{DS\_ON\_MLDO}$(2)	RDS_ON value			40		mΩ
Tx mode						
$V_{IN\_CPOUT\_Tx}$	CP_{OUT} pin input operating voltage range			5	12	V
$V_{IN\_UVLO\_RISING\_Tx}$	Under Voltage Lockout	CP_{OUT} in rising		4.5		V
$V_{IN\_UVLO\_FALLING\_Tx}$	Under Voltage Lockout	CP_{OUT} in falling		3.8		V
$ISNS_{RANGE\_Tx}$	Input Current Sense Range	Trimmed at 1.5A		2		A
Capacitive Divider						
$V_{CPOUT\_RANGE\_BYPASS}$	Bypass voltage range	Bypass Configuration Note 4	3.5		12	V
V_{CPOUT}	Regulated Output Voltage (Bypass Configuration)	V_{RECT} = 5.5V, I_{OUT} = 1.33A	4.7	5	5.3	V
		V_{RECT} = 9.5V, I_{OUT} = 1.33A	8.2	9	9.8	V
		V_{RECT} = 12.5V, I_{OUT} = 1.33A	11.4	12	12.6	V
$V_{CPOUT\_RANGE\_2:1}$[2]	Capacitor Divider voltage range	Capacitor Divider Configuration	6		10	V
V_{CPOUT} [2]	Regulated Output Voltage (Capacitor Divider Configuration)	V_{RECT} = 12.5V, I_{OUT} = 1.33A	5.6	6	6.4	V
		V_{RECT} = 15.5V, I_{OUT} = 1.33A	7.1	7.5	7.9	V
		V_{RECT} = 20.5V, I_{OUT} = 1.33A	9.5	10	10.5	V
V_{CPOUT_STEP}[5]	CPOUT voltage step	Bypass Configuration		100		mV
		Capacitor Divider Config.		50		
$R_{DSON\_CP\_FETs}$	MOSFET R_{DSON}			20		mΩ
$I_{CPOUT\_MAX\_DC}$	Maximum continuous output current	Set $I_{MLDO\_VOUT\_LMT\_RNG}$=1.9A with +/-3%			3	A
I_{CPOUT_ILIM}	Capacitor divider current limit	OCP applied via MLDO ILIM		3.3		A
$f_{SW\_CP\_BUCK\_RNG}$	Switching frequency range	Programmable	0.3	0.6	1.0	MHz
$f_{SW\_CP\_BUCK\_STEP}$	Switching frequency step resolution			11		kHz
$I_{DISCHARGE}$	CPP, CPN, CPOUT discharging resistance			10		mA
$I_{PRE\_CHARGE\_SOURCE}$	CPOUT, CPP pre-charge current source			6		mA
I²C SERIAL INTERFACE(NOTE2)						
V_{IL}	Input Low Threshold	$V_{Pull\text{-}Up}$ = 1.8V		0.7		V
V_{IH}	Input High Threshold			1.4		V
$I_{I2C\_PINS\_LKG}$	Leakage Current	V=1.8V, T_A=25°C		±1		µA
V_{OL}	Output Logic Low	I_{OL}=8mA		0.36		V
f_{SCL}	SCL & SCL_M Clock Frequency	C_b=400pF (max)		400		kHz
C_i	Capacitance for each I/O pin	In f_{SCL}=Max 400kHz		10		pF
$t_{HD,STA}$	Hold Time (Repeated) for START Condition	f_{SCL}=Max 400kHz		0.6		µs
$t_{HD:DAT}$	Data Hold Time			0		µs
t_{LOW}	Low Period of the SCL clock	f_{SCL}=Max 400kHz		1.3		µs

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
t_{HIGH}	High Period of the SCL clock	f_{SCL}=Max 400kHz		0.6		µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition	f_{SCL}=Max 400kHz		0.6		µs
t_{BUF}	Bus Free Time Between STOP and START Condition			1.3		µs
C_b	Capacitive Load for Each Bus Line	f_{SCL}=Max 400kHz		400		pF

NOTE1: The LDO1P8 pin can only be loaded after device startup.
NOTE2: Guaranteed by design and not fully tested in production.
NOTE3: Input voltage operating range is dependent upon the type of transmitter power stage (Full-bridge, half-bridge) and transmitting coil inductance. *WPC Specifications* should be consulted for appropriate input voltage ranges by end-product type.
NOTE4: When Vout is set above 12V, firmware should turn on capacitor divider on into bypass mode with Vout =12V first and then increase the Vout to the final value
NOTE5: Finer step size may be achieved by firmware.

5. Functional Description

5.1 Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters (Tx) that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair (magnetic induction), or over a loosely-coupled inductor pair (magnetic resonance) to a receiver (Rx) in a mobile device. A Wireless Power Consortium (WPC)[1] system uses near field magnetic induction between coils and can be a free-positioning or magnetically-guided type of system.

In WPC systems the amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The Rx-to-Tx communication uses the existing power links (in-band communication) with Amplitude Shift Key (ASK) at 2kbps data rate.

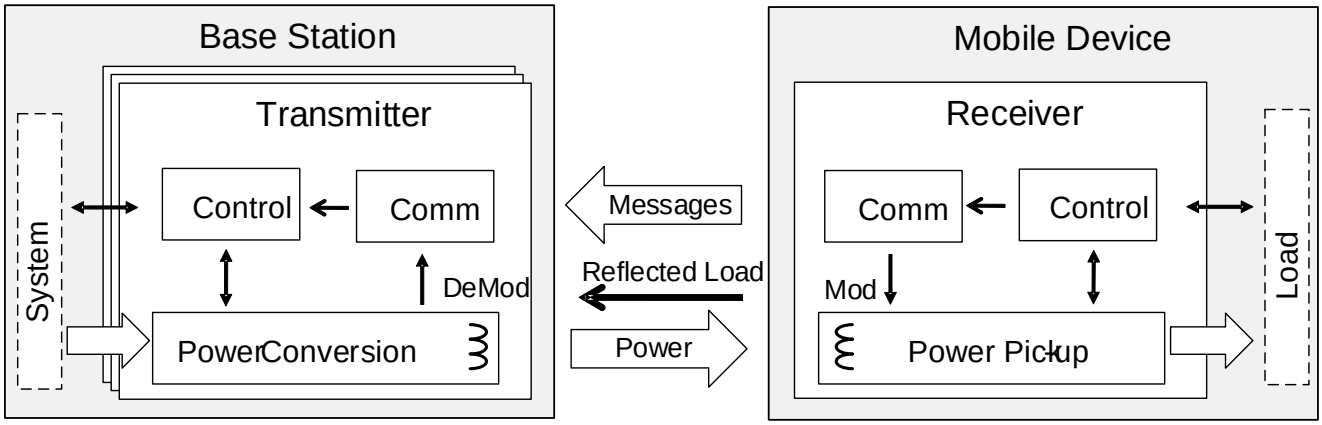

Figure 3. Block Diagram of a WPC System

[1] For the most current information, see the WPC specification at http://www.wirelesspowerconsortium.com/.

5.2 Theory of Operation

5.2.1. Overview

The P9412 is a highly-integrated wireless power transmitter/receiver (TRx) IC for mobile applications. As a wireless power receiver (Rx), the device can deliver up to 30W wirelessly using near-field magnetic induction, and it operates in compliance with WPC specification in all modes. The P9412 also employs higher power protocols enabling the extension of power delivery beyond the WPC EPP standard.

Figure 3 shows the simplified block diagram of the P9412. External Rx coil(s) and CS capacitor(s) transfer energy wirelessly using the P9412 AC1 and AC2 pins to be full-wave-rectified (AC-to-DC).

The wireless power is stored on a capacitor(s) connected to VRECT. Until the voltage across the VRECT capacitor exceeds the UVLO threshold, the rectification is performed by the body diodes of the synchronous full bridge rectifier FETs. After the internal biasing circuit is enabled, the driver and control block operates the MOSFET switches of the rectifier in various modes to maintain reliable connections at optimal efficiency. An internal ADC monitors the voltage at VRECT and the load current, the P9412 sends instructions to the wireless power transmitter to increase or decrease the amount of power transferred or to terminate power transmission based on these readings. The voltage at the output of the P9412 Main Low-Drop-Out (LDO) regulator (VOUT) is programmed from 5V to 20V using I²C commands. The internal temperature is continuously monitored to ensure safe operation.

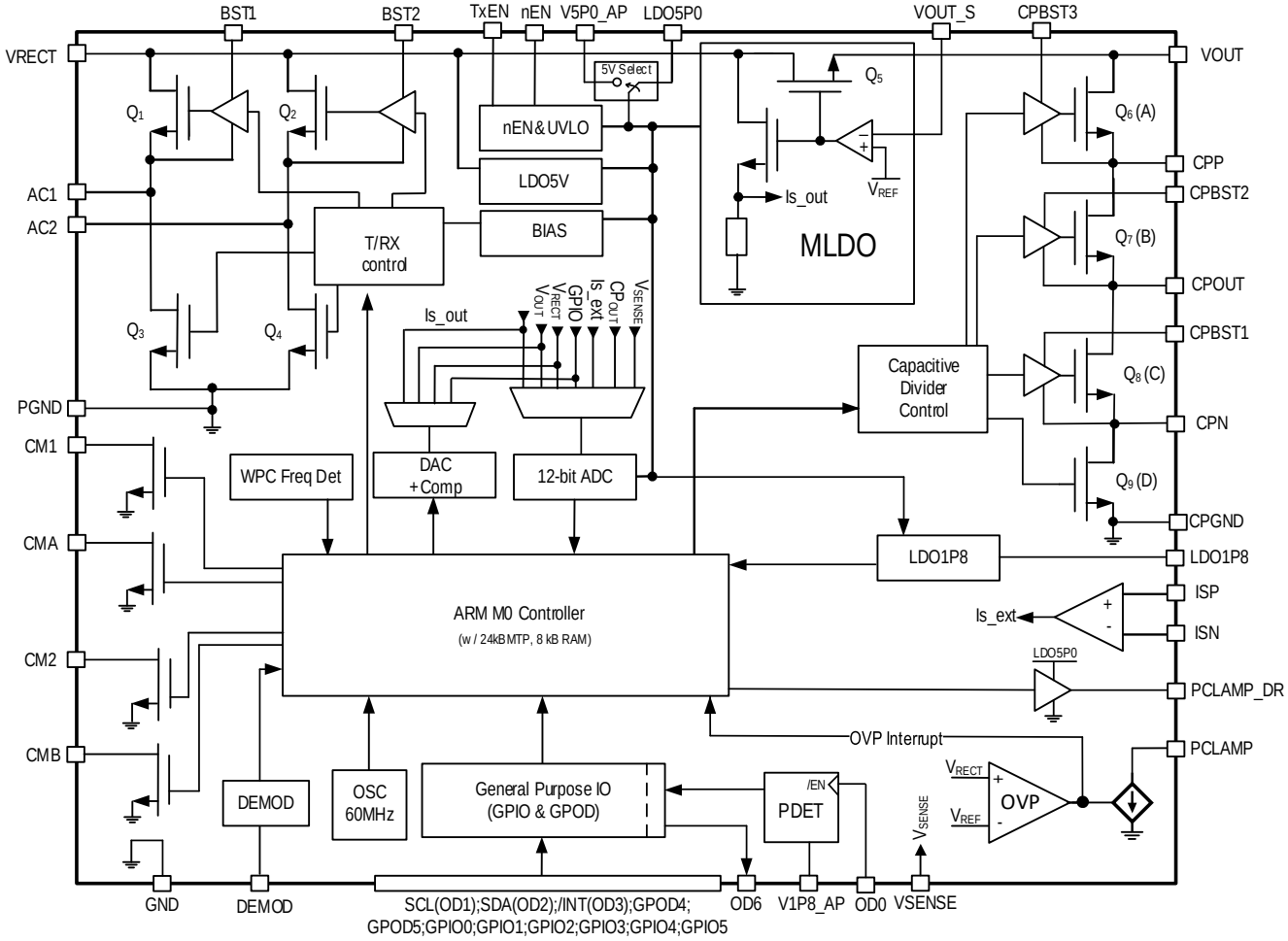

Figure 4. Simplified Block Diagram

5.2.2. Power Control

The voltage at VRECT and the current through the rectifier are sampled periodically and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the internal control logic, which decides whether the loading conditions on VRECT indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at VRECT below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO's load current increases.

5.3 Status and Interrupt Indicators

The P9412 has seven General Purpose Open Drain (GPOD) pins and six General Purpose Input Output (GPIO) pins. The GP pins can be configured to meet a wide variety of signaling and sensing requirements in end applications. The GPIO pins can be push-pull input/outputs and the GPOD pins can be open-drain inputs/outputs. These digital pins are internally biased or referenced to one of the 1.8V voltage rails. The GPIO pins must not be directly connected to GND to avoid overcurrent conditions forced upon the output. Resistive pull-downs on the GPIO pins should be ≥ 2kΩ. When any of the GPOD or GPIO pins are used for analog voltage measurements using the internal ADC, the voltage should be limited to < 1.8V in order to avoid saturating the ADC or forcing a voltage above the reference voltage rail. The most common uses have been designated in the reference schematic and the reference schematic should be followed to align with the latest firmware unless written exception is provided.

5.4 Multiple-Time Programmable Memory

The P9412 includes Multiple-Time Programmable (MTP) memory, or pseudo-flash, that can be re-programmed up to 1000 times. This offers the flexibility of re-programming during pre-production to optimize performance and/or re-programming for field upgrades after product release. The device contains 24kB of MTP memory. The MTP programming voltage range is based on the USB "On-the-Go" (OTG) specification of 5V power (±10%) applied to VRECT via the CP_{OUT} pin.

5.5 Tx Mode

When the P9412 operates as a wireless power transmitter (Tx), power is applied to the VOUT pins as the input, which is the same node as the power receiver (Mobile Device) output when the device operates in WPC Rx Mode. In Tx Mode (Base Station), the Rx is now the Tx and sends instructions that are filtered using the DEMOD filter shown in Figure 5 and decoded internally using a dithered PWM controller for high-resolution voltage modulation decoding. Based on the received packet, the P9412 will adjust the operating frequency to match the transmitted power level to the required receiver power level for reliable and efficient wireless power transfer.

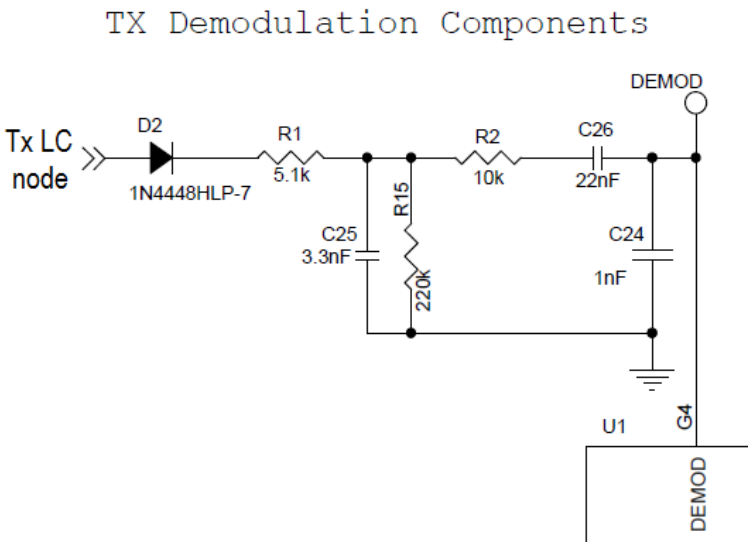

Figure 5. Tx DEMOD Filter and AC Coupling

5.6 Synchronous Rectifier

The efficiency of the full-bridge rectifier in the P9412 is increased by integrating a synchronous rectifier. The rectifier comprises four internally-driven switches that work in a full synchronous mode when the load applied to CP_{OUT} is higher than the programmed threshold value. Below that threshold, the rectifier works in half-synchronous rectification mode. In half-synchronous rectification mode, only the low-side N-MOSFETs are switching and the high-side N-MOSFETs are forced into diode mode. At power-up, when the voltage on V_{RECT} is below the UVLO threshold, the rectifier works by using the MOSFET body diodes to rectify incoming AC voltage to DC voltage. The BST capacitors are used to provide power to drive the gates of the high-side NMOS switches in full-synchronous operating mode.

5.6.1. VRECT Voltage Range

Once VRECT powers up to greater than UVLO, the full-bridge rectifier switches to half-synchronous or full-synchronous mode (based on the loading conditions) to efficiently transfer energy from the transmitter to the load on CP_{OUT}. The control loop of the P9412 maintains the rectifier voltage between 5V and 21.5V, depending on the output current (I_{OUT}) and the programmed output voltage. VRECT must not be directly loaded.

5.6.2. Over-Voltage Protection

In the event that the VRECT voltage increases above the OVP voltage threshold, the P9412 sends an interrupt to the system applications processor (AP), initiates internal self-clamping (PCLAMP), external PCLAMP_DR clamping, and sends control error packets/frequency increment commands to the transmitter in an attempt to bring the rectifier voltage back to a safe operating voltage level. The die temperature is also monitored while simultaneously clamping the incoming energy, and if an over-temperature event occurs, an EPT is sent immediately to the Tx unit. The clamp is released when the VRECT voltage falls below the V_{OVP} hysteresis falling level. If the over-voltage condition persists, an End of Power request is made to the transmitter.

5.7 Over Current, Over-Temperature Protection, and Thermal Shutdown

The P9412 reports over-current (OC) protection and over-temperature (OT) protection by sending an interrupt to the appropriate system AP. Thermal shutdown (TSD) is also supported with “End Power Transfer” packets sent by the P9412 to the transmitter.

The current limit level is set by firmware (FW) and is dependent upon the maximum output current needed (typically 1.5A from the MLDO). If the main LDO (MLDO) output current exceeds the programmed current limit (in Bypass or in Capacitor Divider operating mode) then an OC condition exists and an interrupt is sent to the AP. The MLDO will attempt to limit the output current to the over-current set point by reducing the output voltage proportionally to the amount of current being consumed above the OCP limit. Operating the P9412 in OCP mode will cause CPOUT and VOUT to decrease which will create a voltage difference between Vrect and VOUT and the device temperature will increase. In order to limit the die temperature in over-current conditions, the P9412 may reduce the Vrect target to track VOUT and may send an EPT command to Tx if over-current condition exceeds 0.5s. The host AP is expected to react to the Over-Current interrupt by reducing the load applied to the P9412 immediately. When the output voltage is greater than 15V, over-current conditions can result in rapid heat development and high voltage events which must be limited in time and magnitude to prevent operation under high temperature or prevent exposure to high voltages. The load applied to the P9412 should not be completely removed if on OCP event is active, the load should be reduced to a level within the safe operating output current range. It is recommended that the load reductions should be done in steps (approximately 100mA or 250mA) every 10ms to prevent voltage overshoots caused by rapid load decreases.

The internal device temperature is monitored, and the P9412 reports an over-temperature (OT) condition interrupt to the AP if the temperature exceeds 130°C (typical, internally fixed threshold). The P9412 will generate another interrupt when the temperature falls below the hysteresis level. If the temperature exceeds 140°C (typical), a thermal shutdown (TSD) condition exists and the P9412 will start sending “End Power Transfer” packets with an “over-temperature condition” code until the transmitter stops the power transfer. Power transfer will resume when the transmitter reapplies the ping and the process will repeat.

5.8 Enable Input

The P9412 can be disabled by applying a logic high to the nEN pin. When the nEN pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active. The P9412 should not be disabled at any time during power transfer. In order to use the /EN pin function, wireless power should be terminated via an EPT command, then once power is removed, /EN high can be asserted.

5.9 LDO Regulators

The P9412 has three LDOs, Main LDO (MLDO) and LDO5P0 are powered by VRECT. LDO1P8 is powered by LDO5P0. Both LDO5P0 and LDO1P8 are used to supply power to internal low voltage blocks. The Main LDO output, VOUT, is programmable from 5V to 20V. The LDOs must have local ceramic bypass capacitors placed near the P9412 on the PCB.

5.10 Capacitor Divider

The capacitor divider voltage regulator is a constant frequency (programmable fixed frequency), open-loop switched capacitor divider suitable for high-power and high-voltage applications. In steady state operation, the integrated N-channel MOSFETs are synchronously operated with 50% duty cycle at the pre-programmed switching frequency, and the output voltage is provided at the CP_{OUT} pin. The capacitor divider will output ½ the voltage on VOUT at twice the output current supplied by VOUT. A minimum number of external components are required for proper operation.

5.11 Operating Configurations (Bypass and Capacitor Divider)

The P9412 has three operating configurations: Bypass Mode, Capacitor Divider Mode, and Disable Mode. Upon start-up and connection to a Tx, or in TRx mode, the P9412 will enter Bypass mode (VOUT = CP_{OUT}) and the CP_{OUT} voltage is limited to 3.5V to 12V. Load can be immediately applied at start-up in Bypass mode when CP_{OUT} good interrupt is sent. In order to transition to Capacitor Divider configuration, the P9412 must first enter disable mode in order to start up the capacitor divider. This interim transition mode (Disable) is not user configurable and the P9412 firmware will automatically enter and leave Disable mode when the AP requests a change from Bypass to Capacitor Divider or Capacitor Divider to Bypass configuration. Starting the capacitor divider requires all loading on CP_{OUT} to be removed and then pre-charging the C_{FLY} capacitor and CP_{OUT} capacitor to ½ the VOUT voltage using internal current sources (10mA). The host AP should update the appropriate register after removing the load from CP_{OUT} to initiate configuration changes. The P9412 will not change operating configuration if there is a load applied to CP_{OUT} and an alarm will be issued. After the load is removed and the AP requests the configuration change, the P9412 will automatically start operating in Capacitor Divider mode and signal to the host AP that CP_{OUT} is good and loading may commence. The request to transition between states is handled via I^2C register request, and all settings and control are internally controlled by firmware and are not end-user configurable.

5.12 V5P0AP and V1P8_AP Inputs

In high-power applications where VRECT voltage is expected to be higher than 5V, the power dissipation from the internal 5V LDO is proportional to the difference between the VRECT voltage and LDO5P0 output voltage multiplied by the P9412 active quiescent current plus current required to switch the internal N-FETs. In order to reduce this increasing power loss, an external 5V supply can be provided to the P9412 through the V5P0AP pin. An internal back-to-back FET is connected between the V5P0AP and LDO5P0 pins for isolation.

When using the V5P0_AP pin to reduce power consumption for high output voltage charging, it is recommended to apply the voltage to the pin after power-up, and remove the external power supply before or shortly after wireless power transfer or the connection is terminated. The host AP should enable the V5P0_AP source selection by register when used.

The V1P8_AP input is used to power the integrated Digital Ping Detect circuit and should be connected to the host AP 1.8V power supply so that the Ping Detect function may be used.

5.13 WPC Mode Characteristics

5.13.1. Start-Up

When a mobile device containing the P9412 is placed on a WPC Qi certified charging pad, it responds to the transmitter's "ping" signal by rectifying the AC power from the transmitter and storing it on a capacitor connected to VRECT. During the "Ping" phase, once the rectifier provides voltage at the VRECT pin above the UVLO threshold, the digital section of the P9412 enables communication. The control loop of the P9412 adjusts the rectifier voltage by sending error packets to the transmitter before and after it enables the VOUT MLDO.

The VOUT MLDO is enabled when the power transfer mode is initiated and the voltage at VRECT, the output of the full-wave synchronous rectifier reaches the target voltage that includes headroom in addition to the LDO VOUT target voltage. For example, if the VOUT voltage target is 12 V, the target VRECT voltage is VOUT + headroom, where headroom is a function of the output current. The P9412 Capacitor Divider is set in bypass mode at startup and may be loaded immediately upon power-up. The FW_Inhibit input or the enable pin of the P9412 can be asserted to shut down the P9412 which will disable the entire device and place it in a low current (sleep) mode and the P9412 will not respond to wireless digital ping or send power when in a shutdown state.

5.13.2. Power Transfer

Once the "identification and configuration" phase is completed and successful, "negotiation and calibration" is accomplished then the system enters power transfer mode. The P9412 control circuit measures the rectifier voltage and sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the main LDO linear regulator, and to notify the Tx of the current Rectified Power Packet for Foreign Object Detection (FOD) to guarantee safe efficient power transfer. The P9412 is compatible with WPC (latest specification) and can use compatible Rx or TRx coils. Each receiver coil type has a unique inductance value. As such, a unique resonant capacitance (C_S) may be needed to optimize performance when connected to a given type of receiver coil.

5.13.3. Advanced Foreign Object Detection (FOD) WPC MODE

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of parasitic metal objects are coins, keys, paperclips, etc. The amount of heating depends on the amplitude and frequency of the magnetic field coupled, as well as on the characteristics of the object such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduced power transfer efficiency. Moreover, if no appropriate measures are taken, the heating could lead to unsafe situations if the objects reach high temperatures.

WPC power transmitters and receivers need to also compensate for the power loss due to parasitic metals intentionally designed into the final product – i.e., metals that are neither part of the power transmitter, nor of the power receiver, but which absorb power from magnetic field coupling during power transfer, such as Li-ion batteries, metallic cases, etc.

The P9412 uses advanced FOD techniques to detect foreign objects placed on or near the transmitter base station. The FOD algorithm includes values that are programmable through either the I^2C interface or MTP bits. Programmability is necessary so that the FOD settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the Tx and Rx coils, battery, shielding, and case materials under no load to full load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

The P9412 FOD values need to be tuned prior to production for WPC compliance using final production hardware and coils.

5.13.4. Status/Interrupt Output

When the power transfer connection is established and stable, the VOUT MLDO is enabled. The /INT (GPOD3) should be connected to the AP so that the P9412 can send interrupts to the AP and allow the AP to perform status and interrupt command checks periodically during power transfer. Additional connections from the P9412 to the host AP are recommended as shown in the reference schematic (PDET, SW_Inhibit, and CPout_GD as examples).

5.13.5. WPC Modulation/Communication

The P9412 operates in WPC mode using a single LC tank Rx coil and requires AC modulation capacitor connections for WPC communication. The LC tank should be tuned to achieve maximum efficiency (C_{MA}, C_{MB}, C_{M1}, C_{M2} connected to pins CMA, CMB COM1, COM2) in order to accomplish WPC modulation.

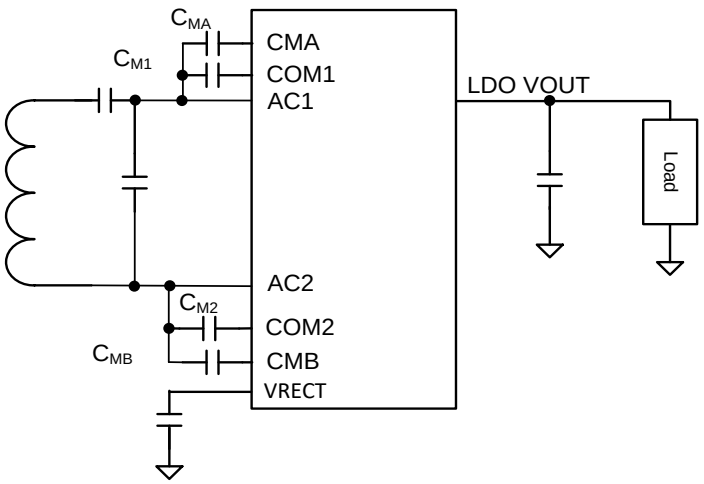

Figure 6. Rx Modulation Components

Receiver-to-transmitter communication is accomplished by modulating the load applied to the receiver's inductor. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. Modulation is done with AC modulation, using internal switches to connect external capacitors from AC1 and AC2 to ground.

The P9412 communicates with the base via communication packets or decodes messages sent by WPC Rx's. Each communication packet has the following structure.

Figure 7. Communication Packet Structure

According to the WPC specification, the power receiver communicates with the power transmitter using backscatter modulation. The load seen by the power transmitter's inductor is modulated on the receiver side to send packets. The power transmitter demodulates these signals as a modulation of coil current/voltage to decode and receive packets.

5.13.6. Bit Encoding Scheme

As required by the WPC, the P9412 uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using two wider transitions as displayed below.

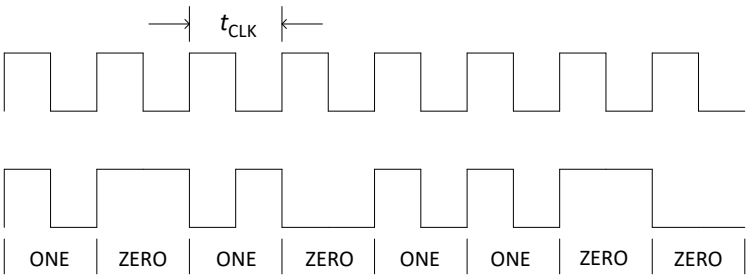

Figure 8. Bit Encoding Scheme

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as displayed below.

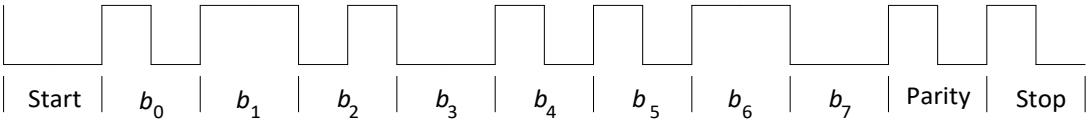

Figure 9. Byte Encoding Scheme

Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

5.13.7. System Feedback Control

The P9412 is fully compatible with the WPC (latest specification), and has all necessary circuitry to communicate with the base station or with a receiver via WPC communication packets. The overall WPC system behavior between the transmitter and receiver follows the state machine shown below.

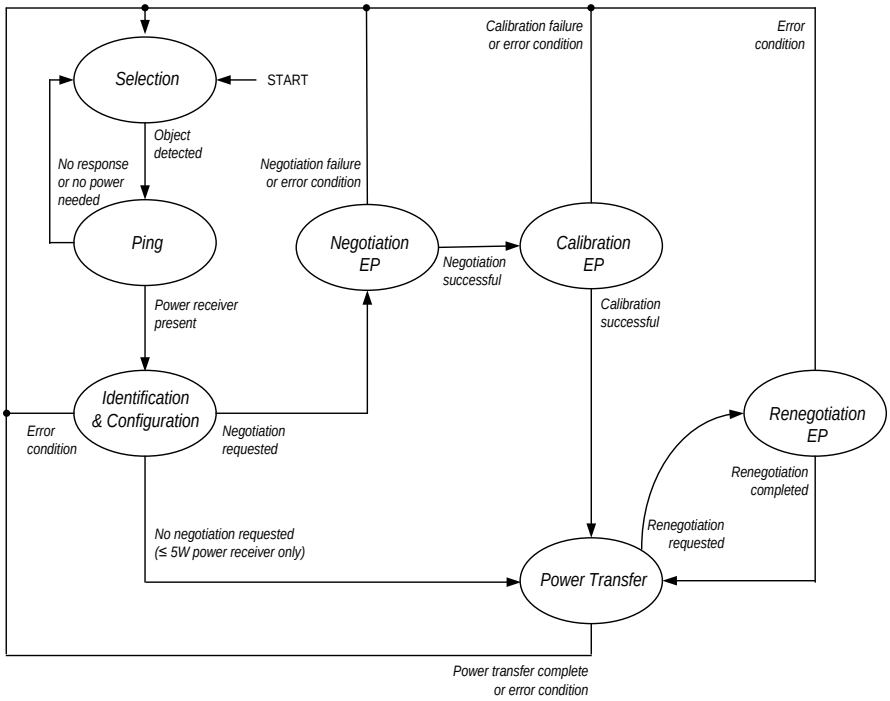

Figure 10. WPC System Feedback Control

The P9412 goes through four phases: Selection, Ping, Identification & Configuration, Negotiation, Calibration and Power Transfer.

5.13.8. Selection

In this phase, the P9412 senses or delivers the wireless power and proceeds to the PING state. It monitors the rectified voltage or DEMOD signal, and when the voltage is above the V_{UVLO_rising} threshold, the P9412 prepares to communicate with the base station or enter power PING mode.

5.13.9. Ping

In this phase, the P9412 transmits a Signal Strength Packet as the first communication packet to instruct the base to keep the power signal ON (or the P9412 detects a Signal Strength Packet). After sending/receiving the Signal Strength Packet, the P9412 proceeds to the Identification and Configuration phase. If, instead, an End of Power Packet is sent or an invalid response is sent, then it remains in the PING phase.

In this phase, the P9412 sends/expects the following packets:

- Signal Strength Packet
- End of Power Packet

5.13.10. Identification and Configuration (ID and Config)

In this phase, the P9412 sends or expect the following packets:

- Identification Packet
- Configuration Packet

After the transmission of the Configuration Packet, the P9412 proceeds to the Negotiation phase.

5.13.11. Negotiation

The Power Receiver negotiates with the Power Transmitter to fine-tune the Power Transfer Contract. For this purpose, the Power Receiver sends negotiation requests to the Power Transmitter, where the Power Transmitter can grant or deny.

5.13.12. Calibration

The Power Receiver provides its Received Power back to the Power Transmitter.

5.13.13. Power Transfer

In this phase, the P9412 controls the power transfer by means of the following Control Data Packets:

- Control Error Packets
- Recieved Power Packets
- End Power Transfer Packet

5.13.14. Renegotiation

In this phase, the Power Receiver can make adjustments to the Power Transfer Contract, if so desired. If necessary, this phase can be aborted prematurely without changing the Power Transfer Contract.

5.13.15. End of Power Transfer (EPT)

In the event of EPT, the P9412 will continuously send End of Power (EPT) packets until the transmitter removes the power and the rectifier voltage on the receiver side drops below the UVLO threshold.

5.14 External Components

The P9412 requires a minimum number of external components for proper operation. For required external components and values and the wiring diagram, see the reference schematic in Figure 16.

5.15 Rx Wireless Power Coil

The Rx coil is dependent on customer requirements since most are custom designs. Renesas recommends the following typical values for Rx-only coils:

Ls = 8 to 10μH
DCR = < 0.3Ω
ACR = < 0.4Ω

For TRx coil design guidance, see Application Note AN-1039 TRx Coil Guide v17. It is recommended to closely follow these coil design guidelines to avoid WPC certification issue's or other power transfer relates obstacles that may lead to delays in production launches caused by improper coupling or unexpected operating conditions.

5.16 Resonance Capacitors

The series resonance capacitors are critical components and must be chosen carefully. All current that flows to the load flows through these components, plus any current lost in the rectifier AC to DC conversion and Capacitive Divider conversion. The recommended capacitor is the 100nF Murata (GRM155R61H104KE19D, 0402, X7R, 50V), which have an ESR ~ 0.1ohms at 100kHz. This capacitor should be selected based on ESR value and DC bias effects. If another capacitor is chosen, inspecting the ESR versus Frequency curve of the manufacturer's capacitor datasheet is necessary to compare ESR characteristics, as well as the DC bias effects on the capacitor value (equivalent or lower ESR and equivalent or higher DC bias at 15V DC applied should be used to select substitutions). Adding an additional non-populated (NP) component placement (C6) is advised if additional capacitance is needed for a particular Rx or TRx coil.

5.17 Input Capacitor (VRECT Capacitors)

The LDO input capacitors (VRECT capacitors) should be located as close as possible to the VRECT pins and ground (PGND). Ceramic capacitors are recommended for their low ESR and small profile. The DC bias effects on the selected capacitors should be considered, and at least 6µF of effective capacitance at 5V DC is recommended for proper device operation for power levels up to 5W. For 10W designs, the effective capacitance should be at least 7.5µF at 10V DC. For 20V output levels, the effective capacitance at 20VDC should be 8µF. A 0.01µF capacitor in a 0201 or 0402 size package is recommended for high frequency decoupling of the VRECT power rail. The voltage rating of these components should be ≥ 35V. Vrect capacitor is the input capacitor for VOUT and is subject to high current events at the wireless power transfer operating frequency.

5.18 Output Capacitors (VOUT and CPOUT Capacitors)

The output capacitor connection to the ground pins (PGND) should be made as short as practical for maximum device performance. Since the LDO has been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance. For better transient response and lower output ripple voltages, the total amount of output capacitance should be increased to meet the output voltage variation target of the application (VRECT capacitance might need to be increased as well). The DC bias effects on the selected capacitors should be considered, and at least 3µF of effective capacitance is required for all output voltages. Additionally to improve performance it is recommended to have 4.5µF of effective capacitance at 10V DC output and 5 µF for 20V DC output levels. A 2.2nF capacitor in a 0201 or 0402 size package is also necessary for high frequency decoupling of the VOUT power rail.

The CP_{OUT} node is a switching capacitive divider output capable of providing 2× the output current supplied by VOUT at ½ the voltage. The Capacitive divider should have a bank of flying capacitors (3 × 22 µF), three bootstrap capacitors and CP_{OUT} bypass capacitors (2 × 10 µF). The output ripple will be a function of the effective capacitance used for C_{FLY} and CP_{OUT} as well as the effective capacitance of Vrect and VOUT. A 1nF capacitor in a 0201 or 0402 size package is recommended for high frequency decoupling of the CP_{OUT} power rail.

5.19 LDO1P8 Capacitor

The P9412 has an internal LDO regulator that must have at least a 1µF to 2.2µF capacitor connected from the LDO1P8 pin to PGND. This capacitor should be as close as possible to the LDO1P8 pin with a close GND connection. A 0.1µF capacitor in a 0201 or 0402 size package can be added for improved high frequency decoupling of the LDO1P8 power rail since this voltage powers the internal ARM Cortex-M0 processor.

5.20 LDO5P0 Capacitor

The P9412 has an internal LDO regulator that must have at least a 1µF to 2.2µF capacitor connected from the LDO5P0 pin to PGND. This capacitor should be as close as possible to the LDO5P0 pin with a close PGND

connection. A 0.1µF capacitor in a 0201 or 0402 size package can be added for improved high-frequency decoupling of the LDO5P0 power rail since this voltage powers the internal ADC, gate drive supplies, and UVLO circuits.

5.21 XY Alignment

The P9412 has integrated XY alignment coil data receive circuitry that should be used to monitor XY alignment coils integrated with the WPC TRx coil. The XY alignment feature allows the device to sense its relative position to the Tx coil magnetic field center and enables FOD compensation to be applied based on the position of the Rx to increase spatial freedom. When used, the XY alignment coils should be connected to pins GP2 (X-alignment coil input) and GP5 (Y-alignment coil input). For more information, see the *P9412 User Manual* and Application Note *P9412 XY Alignment Coil Design, Usage, and Tuning Guide*.

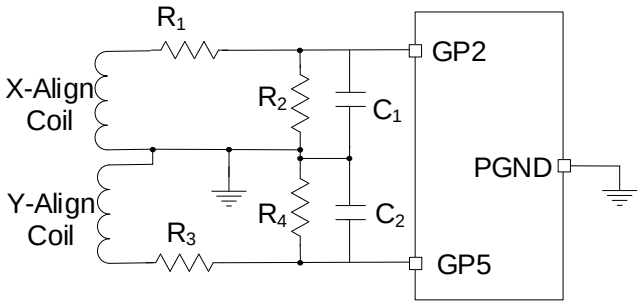

Figure 6. Typical XY Align Coil Schematic Level Connection Guide

5.22 PCLAMP Connection

The P9412 has an internal automatic DC clamping feature to protect the device from events that cause high voltages to occur on the AC or DC side of the rectifier. The clamping engages by the VRECT connection to the PCLAMP pin. The VRECT node must be connected to the PCLAMP pin at all times during Rx mode operation. For greater than 5W operation, the VRECT node is connected to the PCLAMP pin using a 50Ω to 100Ω resistor with greater than 1/4W rating. For space constrained designs, the PCLAMP pin can be directly connected to the VRECT node for 5W or lower power operation. See the *P9412 PCLAMP Application Note* for additional design details and component selection guidance.

5.23 Low Power Ping Detection (PDETB)

Once charging has completed the wireless power connection to the TX can be ended using an End of Power Transfer (EPT) packet to save power. The P9412 can be used to notify the host Application Processor (AP) that it is still on the charging pad by using the PDETB (GPOD6 pin). The PDETB pin must be externally pulled up to the host 1.8V AP power supply rail and will be held low as long as TX PING pulses are detected. If the time interval from the previous digital ping to the next expected digital ping is exceeded the PDETB pin will be released to indicate to the host AP the wireless device has been removed from the Tx charging pad. Proper operation of Ping Detect also requires 1.8V to be applied to V1P8AP and GPOD0 to be pulled- to GND.

5.24 SW Inhibit

The Software (SW) Inhibit input (GPOD5) is used to end power transfer by changing the logic level from low to high at any time. This feature will block the P9412 from performing wireless power transfer when a logic input high is applied to the pin. If the voltage on this pin is changed from low to high during power transfer the P9412 will send EPTs until wireless power is terminated and will no longer respond to digital pings (this can be used to prevent USB and wireless power from simultaneously operating). When the logic level is high TRx mode will also be blocked. The P9412 will operate normally and is always active when this pin is set to a logic low input value.

5.25 Reported Q-Factor (EPP Rx mode)

After the Rx has been placed on an EPP TX the P9412 must report its' Q-Factor to the Tx to check for Open FOD alarm event. The Tx will be responsible for measuring the current quality factor of the Tx coil prior to

connecting to the device and the P9412 will report the typical Q observed by the product. This will be compared to the Tx Q-factor measured value and if within the Tx allowed range charging will commence. If outside the allowable range the Tx will not power the Rx due to suspected presence of a Foreign Object. This feature applies to EPP wireless power protocol and every phone or end product is likely to need some tuning to the reported Quality Factor value. This may be programmed in one of two ways: use of two resistor dividers from LDO1P8 to IO0 and IO1 read-back by ADC or firmware register programmed at the factory (selected by connecting GPIO0 to GND). The simplest and recommended method is to set the value using external resistors read by the ADC at startup to set the reported Q by HW population option (recommended) or the value can be stored in register to be sent to the Tx (requires custom firmware programmed at factory). If the value is stored in register each product must be able to update the MTP register on the manufacturing floor to support device receiver type or model variations. The GPIO0 and GPIO1 pins are the inputs used to select firmware register or hardware selection for reported Q-factor value. The external resistor dividers should be biased by the LDO1P8 power supply to avoid incorrect ADC voltage from being read in the case of a dead battery. See the P9412 User Manual for additional details and population table for determining Q-factor reported values.

5.26 Typical Operating Characteristics

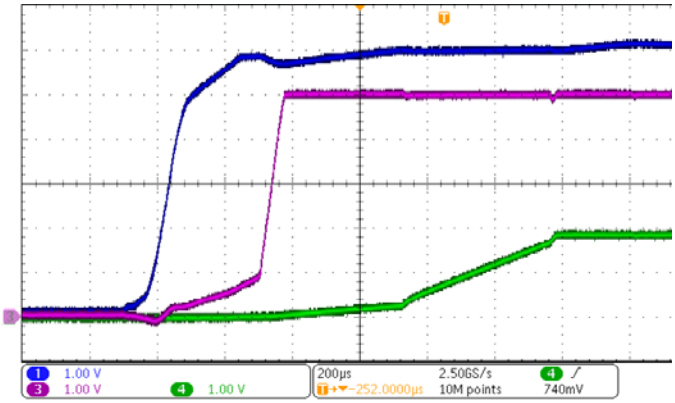

Figure 7. Wireless Initial Start-Up Waveforms Rx Mode from First Digital PING

(ch1=Vrect, ch3=LDO5P0, ch4=LDO1P8)

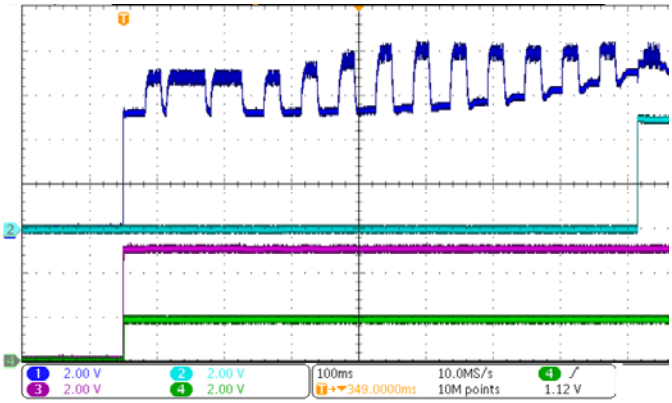

Figure 8. Wireless Start-Up Waveforms Rx Mode from First Digital PING until VOUT

ch1=Vrect, ch2=Vout, ch3=LDO5P0, ch4=LDO1P8

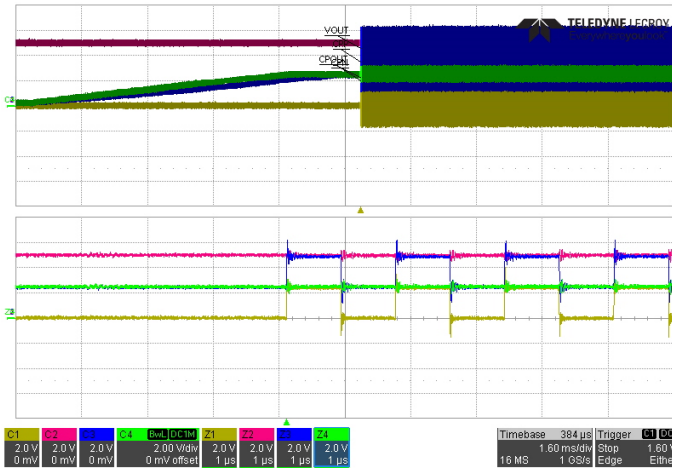

Figure 9. Capacitive Divider Start-up Waveforms (Initiated after Wireless Power Start-Up), VOUT=6V

(ch1=CPN, ch2=VOUT, ch3=CPP, ch4=CPOUT8)

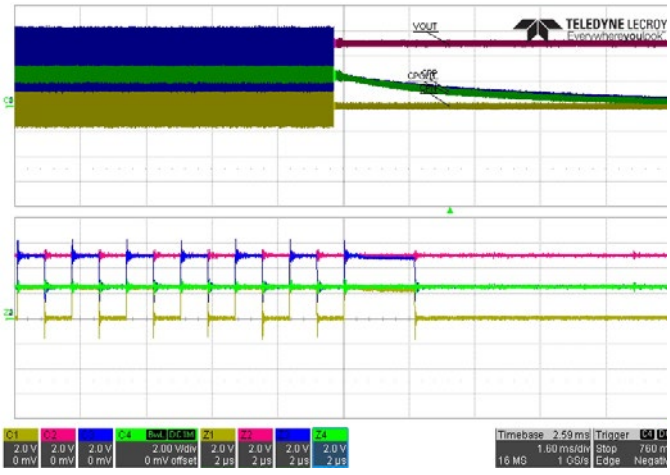

Figure 10. Capacitive Divider Shutdown Waveforms (Initiated after Wireless Power Start-Up), VOUT=6V

(ch1=CPN, ch2=VOUT, ch3=CPP, ch4=CPOUT8)

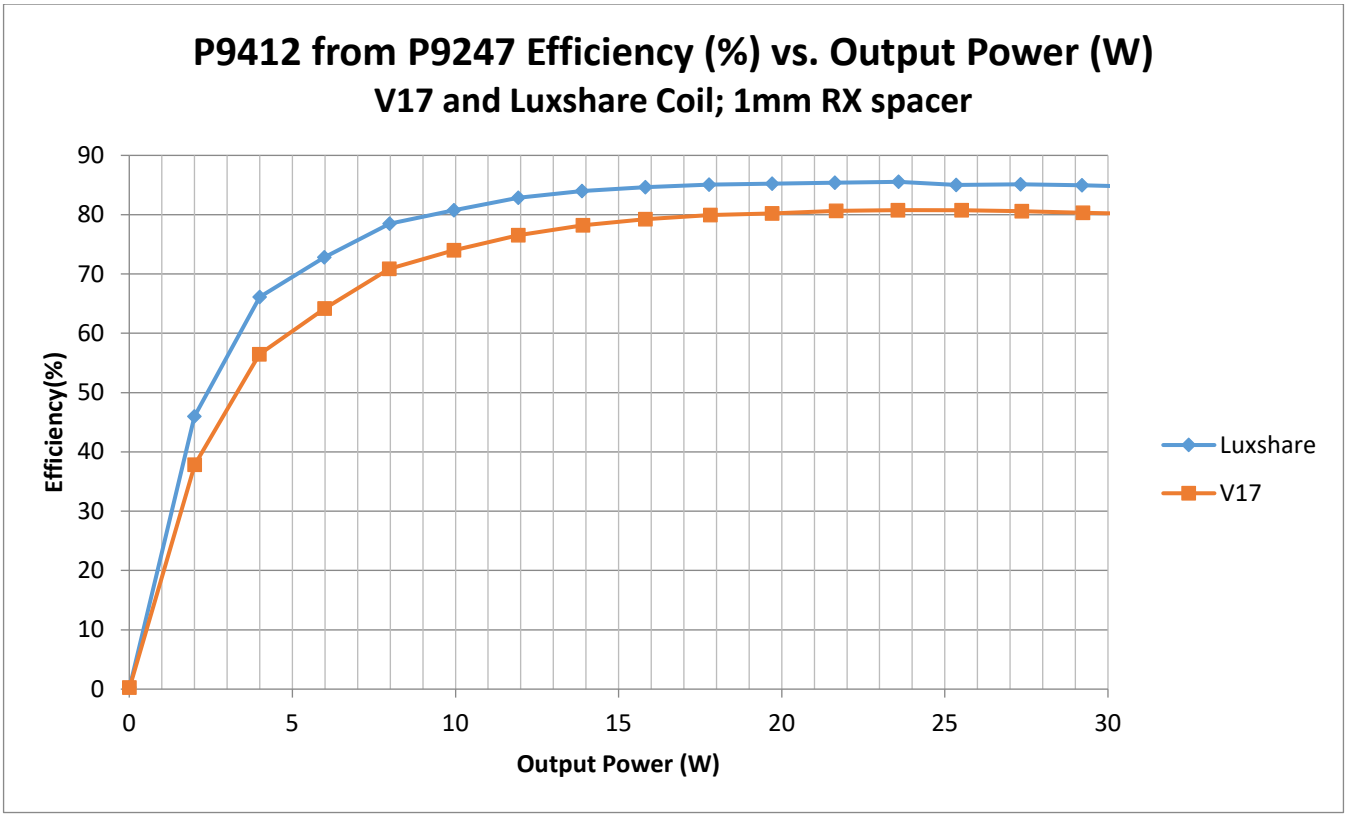

Figure 11. WP Efficiency vs. Output Current; Capacitor Divider Mode at 10V 0 to 30W, various Rx Coils

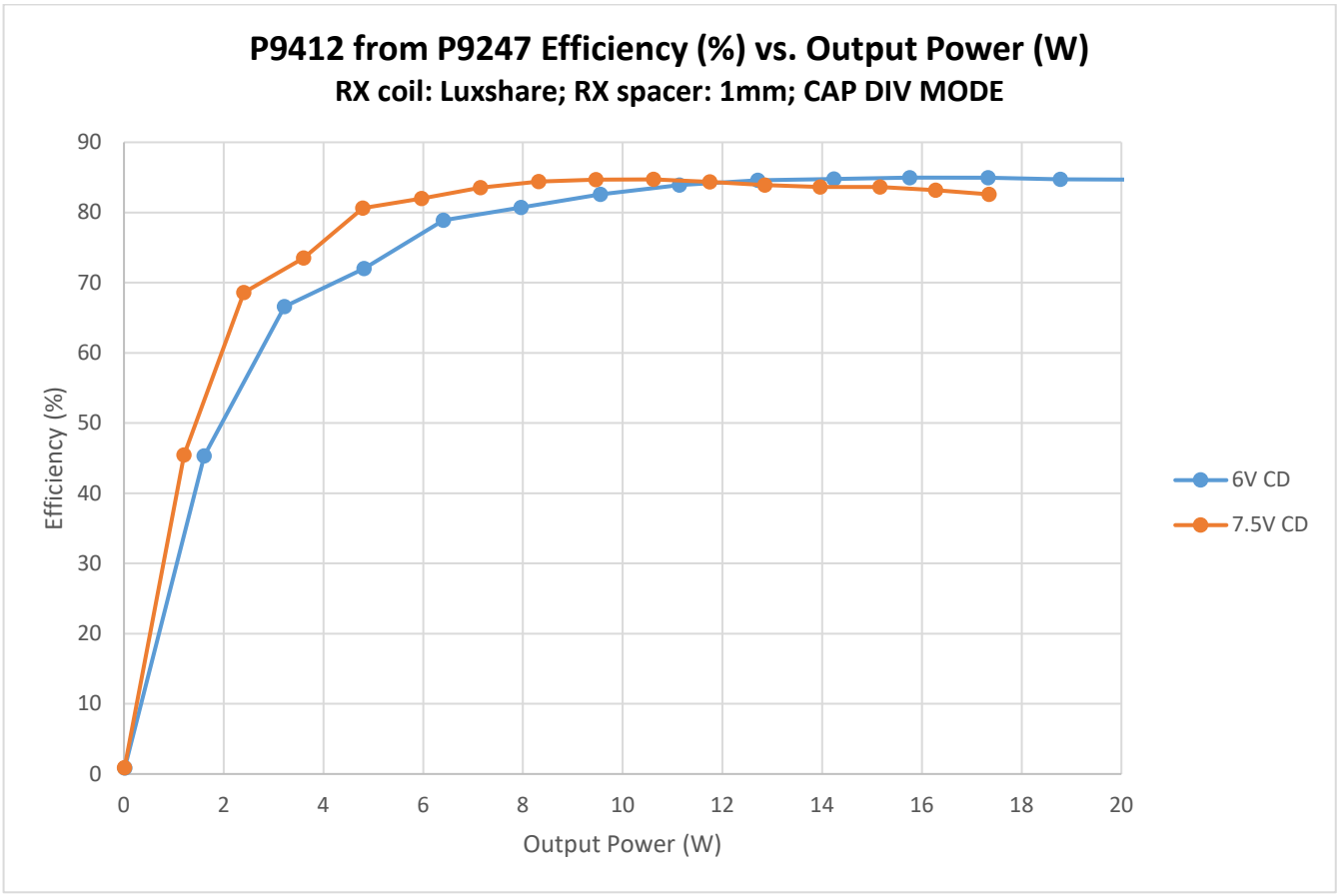

Figure 12. WP Efficiency vs. Output Current; Capacitor Divider Mode at 6V, 7.5V with Rx only Coil

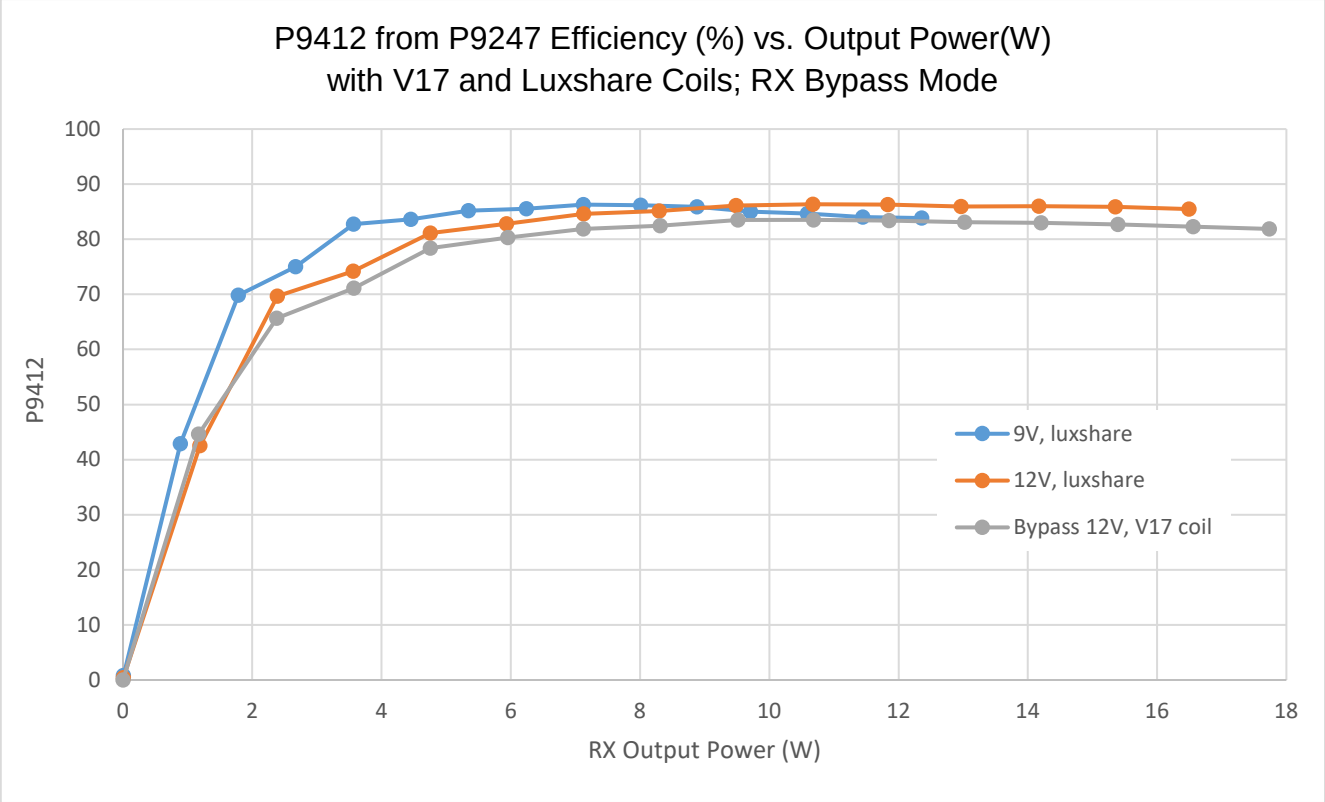

Figure 13. Efficiency vs. Output Current during Wireless Power Transfer; Bypass Mode (VOUT=CPOUT)

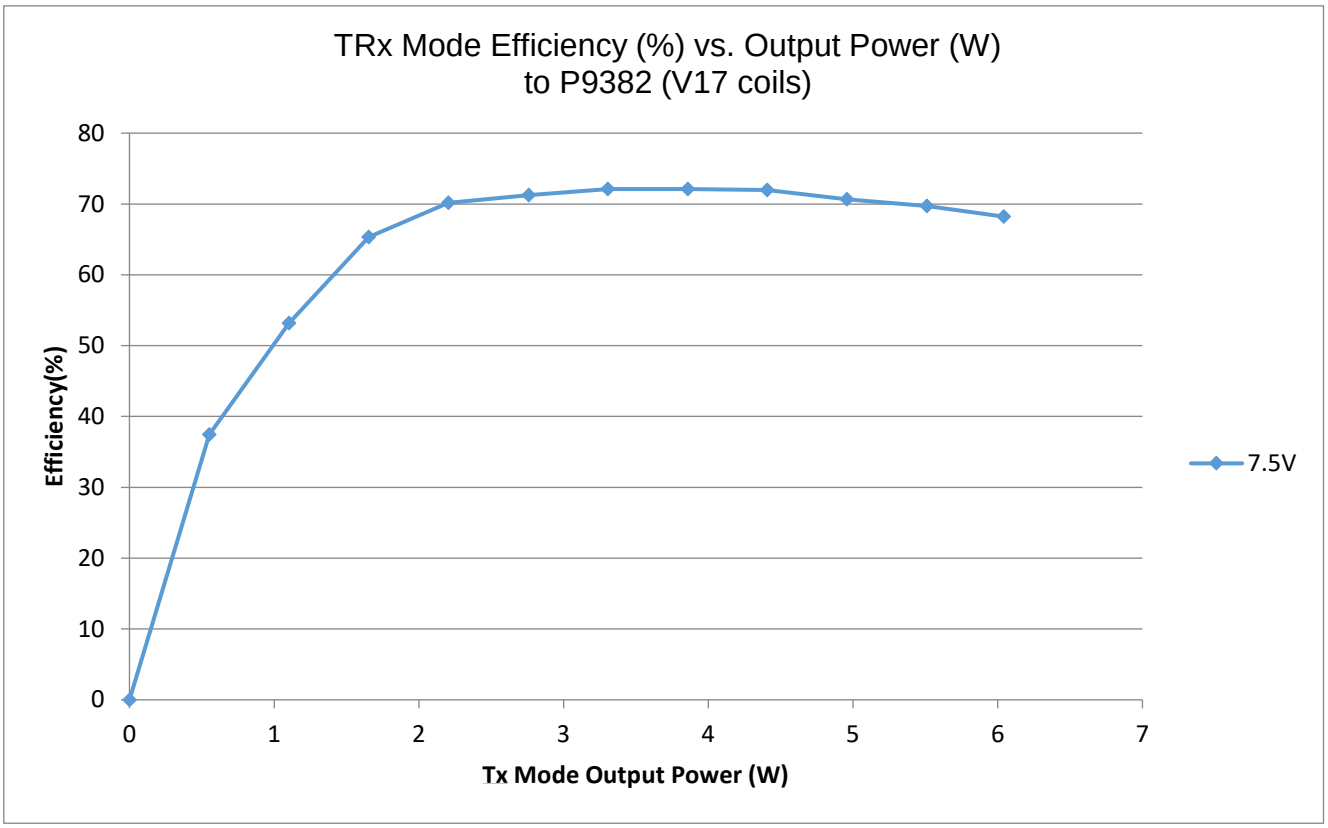

Figure 14. Efficiency vs. Output Current during Wireless Power transfer; Tx Mode (VIN=CPOUT)

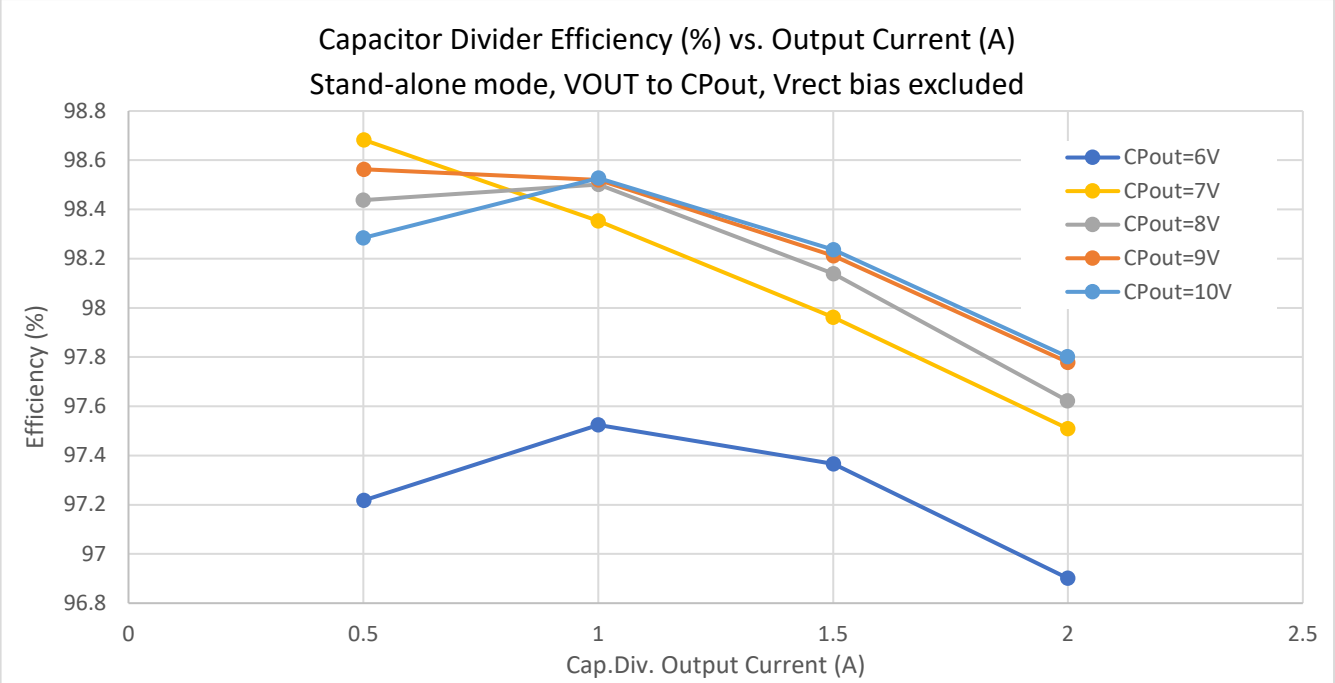

Figure 15. Efficiency vs. Output Current Stand-alone Capacitor Divider Only (VOUT=Vrect=2xCPout)

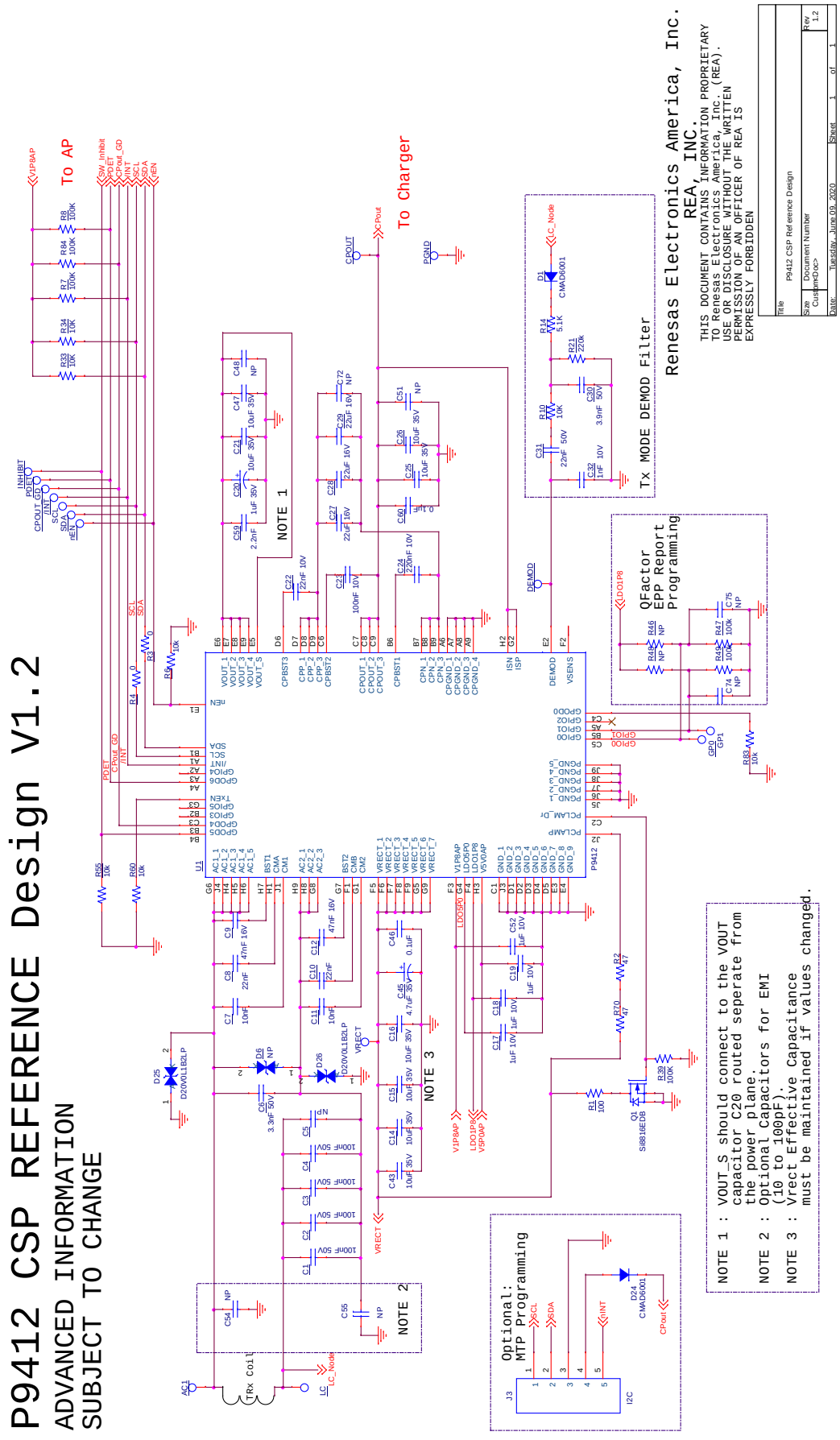

Figure 16. P9412 CSP DEMO PCB Reference Schematic

6. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/81-dsbga-package-outline-drawing-402-x-401-x-05-mm-body-04mm-pitch-awq81d1

7. Ordering Information

Orderable Part Number	Description	Shipping Packaging	Temperature	Firmware Contents
P9412-0AWQI8	WLCSP 4.02 × 4.01 × 0.50 mm 0.40mm Pitch	Reel	-40°C to +85°C	Blank

8. Revision History

Revision	Date	Description
1.1	Nov.4.20	Updated the ordering information.
1.0	June 10.20	Initial release.

81-DSBGA, Package Outline Drawing

4.02 x 4.01 x 0.5 mm Body, 0.4mm Pitch

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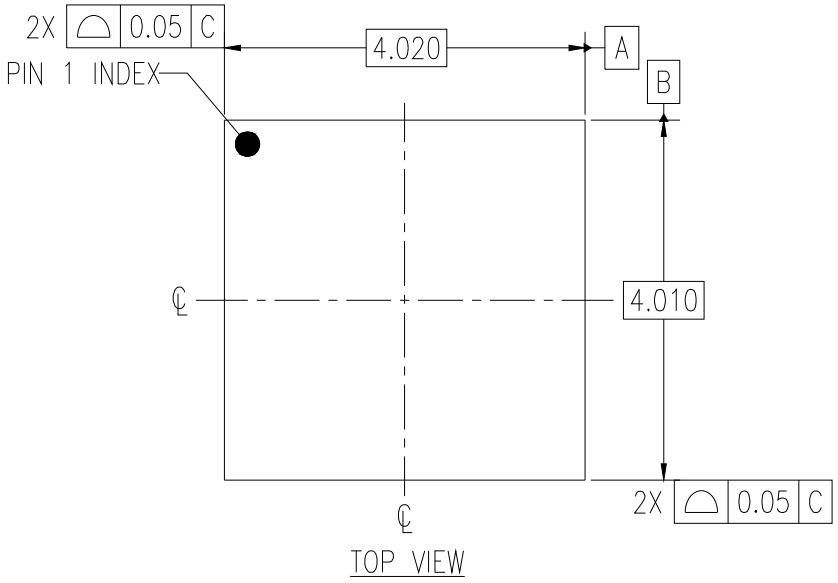
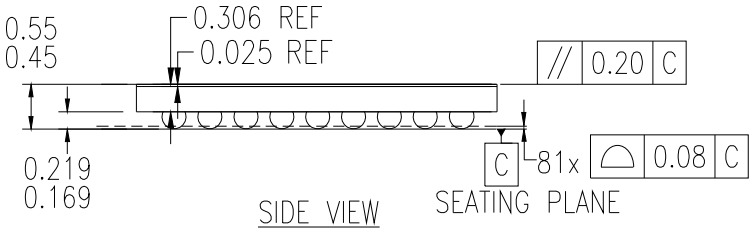
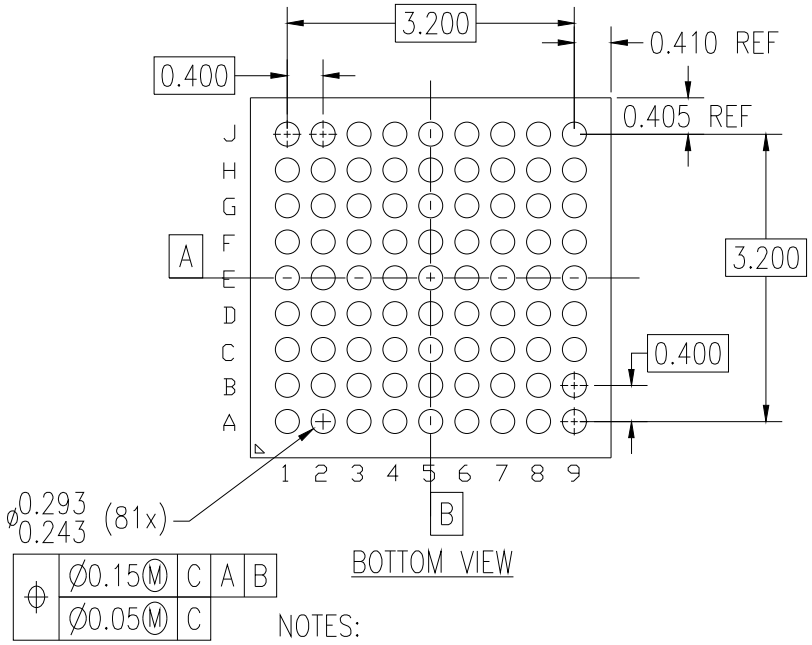


TOP VIEW



SIDE VIEW

SEATING PLANE



BOTTOM VIEW

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. DIE STEP SIZE 4.06 x 4.05 MM.