User's Manual

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RH850/F1KM

User's Manual: Hardware

Renesas microcontroller
RH850 Family

Addendum for ISELED

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Rev.1.10 June, 2023

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(Rev.5.0-1 October 2020)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The part names of the additional products are shown in this document including the correspondence table between the general products and the additional products. The specification of additional products is the same as the general product except the specification items shown in this document.

The following documents apply to the RH850/F1KM Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RH850/F1KH, RH850/F1KM User's Manual: Hardware	R01UH0684EJxxxx

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representation: xxx (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on the bottom

Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numeric representation: Binary ... xxxx or $xxxx_B$

Decimal ... xxxx

Hexadecimal ... $xxxx_H$

Prefix indicating power of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

G (giga): $2^{30} = 1,024^3$

Description of Registers

Each register description includes register access, register address, and register value after a reset, a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meaning of the bit settings.

The standard format for bit charts and tables are described below.

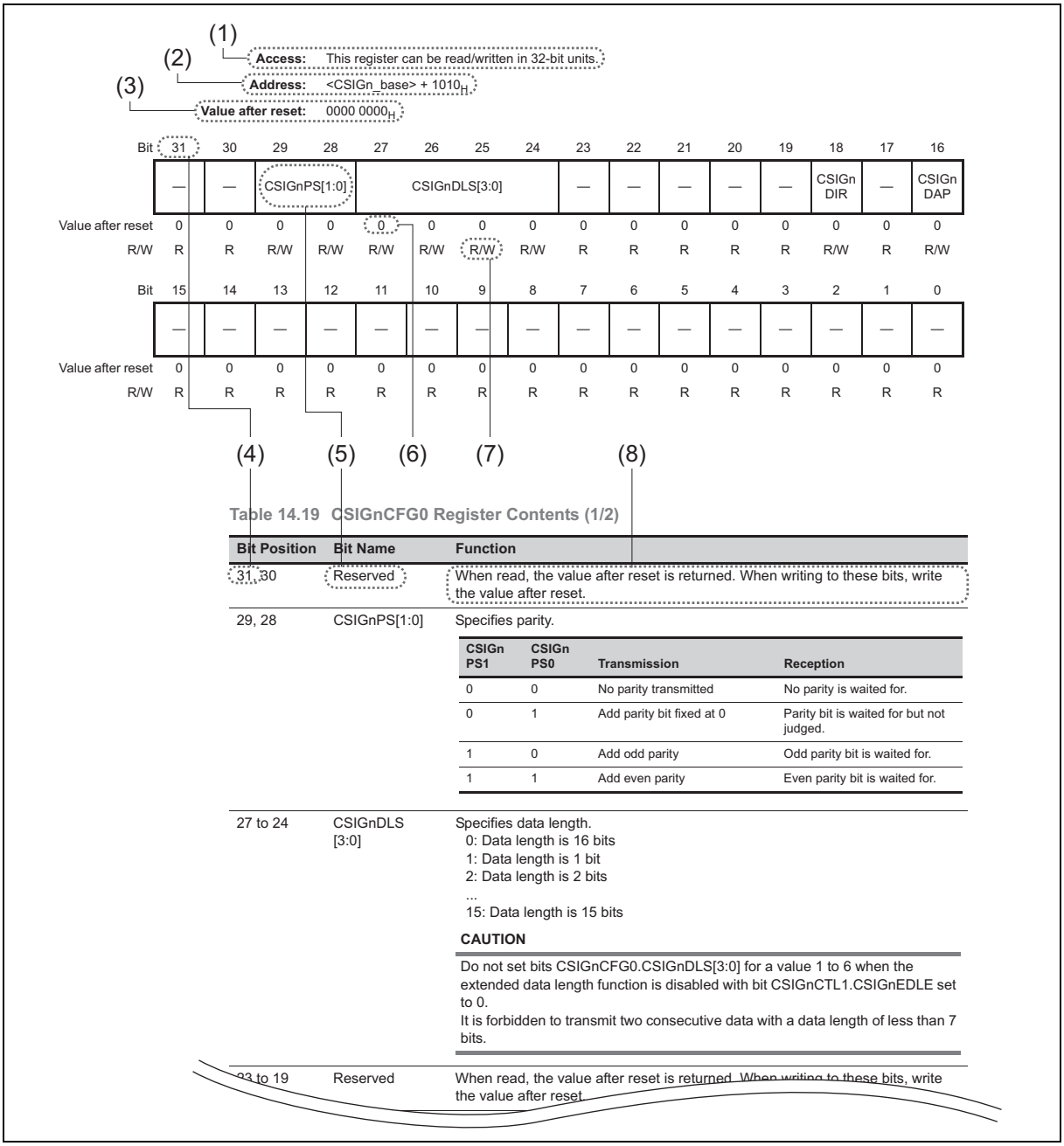

Table 14.19 CSIGnCFG0 Register Contents (1/2)

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
29, 28	CSIGnPS[1:0]	Specifies parity.
27 to 24	CSIGnDLS [3:0]	Specifies data length. 0: Data length is 16 bits 1: Data length is 1 bit 2: Data length is 2 bits ... 15: Data length is 15 bits
23 to 19	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.

CSIGn PS1	CSIGn PS0	Transmission	Reception
0	0	No parity transmitted	No parity is waited for.
0	1	Add parity bit fixed at 0	Parity bit is waited for but not judged.
1	0	Add odd parity	Odd parity bit is waited for.
1	1	Add even parity	Even parity bit is waited for.

CAUTION

Do not set bits CSIGnCFG0.CSIGnDLS[3:0] for a value 1 to 6 when the extended data length function is disabled with bit CSIGnCTL1.CSIGnEDLE set to 0.
It is forbidden to transmit two consecutive data with a data length of less than 7 bits.

(1) Access

The register can be accessed in the bit unit indicated here.

(2) Address

This is the register address.
For base address, see description of base address in each section.

(3) Value after a reset (in hexadecimal notation)

This is the value of all bits of the register after a reset. Values for bytes are given as numbers in the range from 0 to 9 and letters from A to F or as X where they are undefined.

(4) Bit position

This is the bit number.
The bits are numbered from 31 to 0 for 32-bit registers, 15 to 0 for 16-bit registers, and 7 to 0 for 8-bit registers.

(5) Bit name

Bit name or field name is indicated.
When clearly identifying the digits of a bit field is required, do so by using a form such as CSIGnDLS[3:0] above.
Indicate reserved bits by using a dash (—).

(6) Value after a reset (in binary notation)

This is the bit values after a reset.

0	:	The value after a reset is 0.
1	:	The value after a reset is 1.
—	:	The value after a reset is undefined.

(7) R/W

This is the bit attribute of all bits of the register.

R/W	:	The bit or field is readable and writable.
R	:	The bit or field is readable. Note that all reserved bits are indicated as R. When written, the value specified in the bit chart or the value after a reset should be written. In case of writing to writable registers that also include non-reserved bits with the R-attribute, writing to the R-attribute bits will be ignored unless otherwise specified.
W	:	This bit or field is writable. When read, the value is undefined. If a value is indicated in the bit chart, the value is returned.

(8) Function

This is function of the bit.

Section 1 Overview

1.1 Product Lineup

The specification of additional products is the same as the general product except the specification items shown in this document.

Table 1.1 Product Lineup of RH850/F1KM-S1

Series	Pin Count	CPU frequency	Code Flash	Data Flash	Local RAM	Retention RAM	Trace RAM	Operating temperature (Ta)	Part Name (General product)	Part Name (Additional product)
F1KM-S1	100pin	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	–40°C to +105°C	R7F7016843AFP-C LQFP	R7F701A643AFP-C LQFP
			768 KB		64 KB		Not available		R7F7016853AFP-C LQFP	R7F701A653AFP-C LQFP
			512 KB		32 KB		Not available		R7F7016863AFP-C LQFP	R7F701A663AFP-C LQFP
	80pin	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	–40°C to +105°C	R7F7016873AFP-C LQFP	R7F701A673AFP-C LQFP
			768 KB		64 KB		Not available		R7F7016883AFP-C LQFP	R7F701A683AFP-C LQFP
			512 KB		32 KB		Not available		R7F7016893AFP-C LQFP	R7F701A693AFP-C LQFP
	64pin	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	–40°C to +105°C	R7F7016903AFP-C LQFP	R7F701A703AFP-C LQFP
			768 KB		64 KB		Not available		R7F7016913AFP-C LQFP	R7F701A713AFP-C LQFP
			512 KB		32 KB		Not available		R7F7016923AFP-C LQFP	R7F701A723AFP-C LQFP
	48pin	120 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	–40°C to +105°C	R7F7016933AFP-C LQFP	R7F701A733AFP-C LQFP
			768 KB		64 KB		Not available		R7F7016943AFP-C LQFP	R7F701A743AFP-C LQFP
			512 KB		32 KB		Not available		R7F7016953AFP-C LQFP	R7F701A753AFP-C LQFP

Table 1.2 Product Lineup of RH850/F1KM-S2

Series	Pin Count	CPU frequency	Code Flash	Data Flash	Local RAM	Global RAM (GRAM)	Retention RAM	Trace RAM	Operating temperature (Ta)	Part Name (General product)	Part Name (Additional product)
F1KM-S2	100pin	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	–40°C to +105°C	R7F7017603AFP-C LQFP	R7F701A783AFP-C LQFP
	144pin	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	–40°C to +105°C	R7F7017623AFP-C LQFP	R7F701A773AFP-C LQFP
	176pin	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	–40°C to +105°C	R7F7017643AFP-C LQFP	R7F701A763AFP-C LQFP

Table 1.3 Product Lineup of RH850/F1KM-S4

Series	Pin Count	CPU frequency	Code Flash	Data Flash	Local RAM	Global RAM (GRAM)	Retention RAM	Trace RAM	Operating temperature (Ta)	Part Name (General product)	Part Name (Additional product)
F1KM-S4	100pin	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	–40°C to +105°C	R7F7016443AFP-C LQFP	R7F701A843AFP-C LQFP
			4 MB		256 KB	192 KB		32 KB		R7F7016453AFP-C LQFP	R7F701A833AFP-C LQFP
	144pin	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	–40°C to +105°C	R7F7016463AFP-C LQFP	R7F701A823AFP-C LQFP
			4 MB		256 KB	192 KB		32 KB		R7F7016473AFP-C LQFP	R7F701A813AFP-C LQFP
	176pin	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	–40°C to +105°C	R7F7016483AFP-C LQFP	R7F701A803AFP-C LQFP
			4 MB		256 KB	192 KB		32 KB		R7F7016493AFP-C LQFP	R7F701A793AFP-C LQFP

Section 2 Flash Memory

2.1 Reading Flash Memory

2.1.1 Reading Data Flash Memory

2.1.1.1 PRDNAMEn — Product Name Storage Register (n = 1 to 3)

This register stores the product name. The product part name is stored in 16-byte ASCII code, and PRDNAME1, PRDNAME2, and PRDNAME3 correspond to the fourth to first bytes, eighth to fifth bytes, and twelfth to ninth bytes of the product part name respectively.

Access: These registers are read-only registers that can be read in 32-bit units.

Address: PRDNAME1: FFCD 00D0$_H$

PRDNAME2: FFCD 00D4$_H$

PRDNAME3: FFCD 00D8$_H$

Value after reset: See Table 2.2, Table 2.3 and Table 2.4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRDNAMEn[31:24]*1								PRDNAMEn[23:16]*1							
Value after reset																
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRDNAMEn[15:8]*1								PRDNAMEn[7:0]*1							
Value after reset																
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note 1. n = 1 to 3.

Table 2.1 PRDNAMEn Register Contents

Bit Position	Bit Name	Function
31 to 24	—	Product name fourth byte (PRDNAME1), eighth byte (PRDNAME2) twelfth byte (PRDNAME3)
23 to 16	—	Product name third byte (PRDNAME1), seventh byte (PRDNAME2) eleventh byte (PRDNAME3)
15 to 8	—	Product name second byte (PRDNAME1), sixth byte (PRDNAME2) tenth byte (PRDNAME3)
7 to 0	—	Product name first byte (PRDNAME1), fifth byte (PRDNAME2) ninth byte (PRDNAME3)

Table 2.2 List of Registers Related to Product Information (RH850/F1KM-S1)

Product Part Name	PRDNAME1	PRDNAME2	PRDNAME3
R7F701A64	3746 3752	3641 3130	2020 2034
R7F701A65	3746 3752	3641 3130	2020 2035
R7F701A66	3746 3752	3641 3130	2020 2036
R7F701A67	3746 3752	3641 3130	2020 2037
R7F701A68	3746 3752	3641 3130	2020 2038
R7F701A69	3746 3752	3641 3130	2020 2039
R7F701A70	3746 3752	3741 3130	2020 2030
R7F701A71	3746 3752	3741 3130	2020 2031
R7F701A72	3746 3752	3741 3130	2020 2032
R7F701A73	3746 3752	3741 3130	2020 2033
R7F701A74	3746 3752	3741 3130	2020 2034
R7F701A75	3746 3752	3741 3130	2020 2035

Table 2.3 List of Registers Related to Product Information (RH850/F1KM-S2)

Product Part Name	PRDNAME1	PRDNAME2	PRDNAME3
R7F701A78	3746 3752	3741 3130	2020 2038
R7F701A77	3746 3752	3741 3130	2020 2037
R7F701A76	3746 3752	3741 3130	2020 2036

Table 2.4 List of Registers Related to Product Information (RH850/F1KM-S4)

Product Part Name	PRDNAME1	PRDNAME2	PRDNAME3
R7F701A84	3746 3752	3841 3130	2020 2034
R7F701A83	3746 3752	3841 3130	2020 2033
R7F701A82	3746 3752	3841 3130	2020 2032
R7F701A81	3746 3752	3841 3130	2020 2031
R7F701A80	3746 3752	3841 3130	2020 2030
R7F701A79	3746 3752	3741 3130	2020 2039

RH850/F1KM
User’s Manual: Hardware

Publication Date: Rev.1.10 June 30, 2023

Published by: Renesas Electronics Corporation

RH850/F1KM

Renesas Electronics Corporation

R01UH1042EJ0110