User's Manual

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μPD78F802x, 78F803x Microcontrollers

User's Manual: Hardware

RENESAS MCU
78F802x, 78F803x Microcontrollers

μPD78F8026(A)
μPD78F8027(A)
μPD78F8028(A)
μPD78F8029(A)
μPD78F8030(A)
μPD78F8032D
μPD78F8033(A)
μPD78F8034(A)
μPD78F8035(A)
μPD78F8036(A)
μPD78F8037(A)
μPD78F8039D

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD78F802x, 78F803x microcontrollers, and to design and develop application systems and programs for these devices.

<R>
- μPD78F802x, 78F803x microcontroller (48-pin products) :
  μPD78F8026(A), 78F8027(A), 78F8028(A), 78F8029(A), 78F8030(A), 78F8032D
- 78F803x microcontroller (64-pin products) :
  μPD78F8033(A), 78F8034(A), 78F8035(A), 78F8036(A), 78F8037(A), 78F8039D

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD78F802x, 78F803x microcontrollers manuals are separated into three manuals: this manual, 78K0/Kx2 User's Manual, 78K0/Kx2 ROM Expansion Products User's Manual, and the Instructions edition (common to the 78K0 Series).

μPD78F802x, 78F803x Microcontroller User's Manual (This Manual)	**78K0/Kx2 User's Manual**	**78K0/Kx2 ROM Expansion Products User's Manual**
• Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications (target)	• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU architecture • Memory bank select function • Multiplier/divider • Flash memory

78K/0 Series User's Manual Instructions
• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**.

<R>
- When using this manual as the manual for (A) grade products of the μPD78F802x, 78F803x microcontrollers:
  → Only the quality grade differs between standard products and (A), grade products. Read the part number as follows.

- μPD78F8026 → μPD78F8026(A)
- μPD78F8027 → μPD78F8027(A)
- μPD78F8028 → μPD78F8028(A)
- μPD78F8029 → μPD78F8029(A)
- μPD78F8030 → μPD78F8030(A)
- μPD78F8033 → μPD78F8033(A)
- μPD78F8034 → μPD78F8034(A)
- μPD78F8035 → μPD78F8035(A)
- μPD78F8036 → μPD78F8036(A)
- μPD78F8037 → μPD78F8037(A)

- To know details of the microcontroller part:
  → Refer to the separate document **78K0/Kx2 User's Manual (R01UH0008E)** and **78K0/Kx2 ROM Expansion Products User's Manual (U19719E)**.

78K0/KB2 microcontroller products	The products corresponding to the 78K0/KB2 microcontroller products
μPD78F0501A	μPD78F8026
μPD78F0502A	μPD78F8027
μPD78F0503A	μPD78F8028
μPD78F0504A	μPD78F8029
μPD78F0505A	μPD78F8030
μPD78F0507DA	μPD78F8032D

78K0/KC2 microcontroller products	The products corresponding to the 78K0/KC2 microcontroller products
μPD78F0511A	μPD78F8033
μPD78F0512A	μPD78F8034
μPD78F0513A	μPD78F8035
μPD78F0514A	μPD78F8036
μPD78F0515A	μPD78F8037
μPD78F0517DA	μPD78F8039D

- To know details of the 78K0 microcontroller instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD78F802x, 78F803x Microcontrollers User's Manual	This Manual
78K0/Kx2 User's Manual	R01UH0008E
78K0/Kx2 ROM Expansion Products User's Manual	U19719E
78K/0 Series Instructions User's Manual	U12326E
78K0/Kx2 Flash Memory Programming (Programmer) Application Note	U17739E
78K0 Microcontrollers Self Programming Library Type01 User's Manual	U18274E
78K0 Microcontrollers EEPROM™ Emulation Library Type01 User's Manual	U18275E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-78K0KX2 In-Circuit Emulator	U17341E
QB-MINI2 On-Chip Debug Emulator with Programming Function	R20UT0449E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Ver.3.80 Assembler Package User's Manual Note 1	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
78K0 Assembler Package RA78K0 Ver.4.01 Operating Precautions (Notification Document) Note 1		ZUD-CD-07-0181-E
CC78K0 Ver.3.70 C Compiler User's Manual Note 2	Operation	U17201E
	Language	U17200E
78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions (Notification Document) Note 2		ZUD-CD-07-0103-E
ID78K0-QB Ver.2.94 Integrated Debugger User's Manual	Operation	U18330E
ID78K0-QB Ver.3.00 Integrated Debugger User's Manual	Operation	U18492E
PM plus Ver.5.20 Note 3 User's Manual		U16934E
PM+ Ver.6.30 Note 4 User's Manual		U18416E

Notes 1. This document is installed into the PC together with the tool when installing RA78K0 Ver. 4.01. For descriptions not included in "78K0 Assembler Package RA78K0 Ver. 4.01 Operating Precautions", refer to the user's manual of RA78K0 Ver. 3.80.

2. This document is installed into the PC together with the tool when installing CC78K0 Ver. 4.00. For descriptions not included in "78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions", refer to the user's manual of CC78K0 Ver. 3.70.

3. PM plus Ver. 5.20 is the integrated development environment included with RA78K0 Ver. 3.80.

4. PM+ Ver. 6.30 is the integrated development environment included with RA78K0 Ver. 4.01. Software tool (assembler, C compiler, debugger, and simulator) products of different versions can be managed.

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	R20UT0008E

Other Documents

Document Name	Document No.
<R> RENESAS MICROCOMPUTER GENERAL CATALOG	R01CS0001E
Semiconductor Device Mount Manual	**Note**
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Review of Quality and Reliability Handbook Information	R51ZZ0001E

Note See the "Semiconductor Device Mount Manual" website
<R> (http://www.renesas.com/products/package/manual/index.jsp).

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Table of Contents

CHAPTER 1 OUTLINE

μPD78F802x and 78F803x microcontrollers are MCP (Multi-Chip Package) which combined 2 chips in 1 package: an analog chip (including LIN transceiver, power supply, and high side driver) and 8-bit microcontroller chip.

The 8-bit microcontroller blocks of the μPD78F802x and 78F803x are mounted with the 78K0/KB2 and 78K0/KC2, respectively.

1.1 Features

○ ROM, RAM capacities

ROM[Note]	High-Speed RAM[Note]	Expansion RAM[Note]	48 pins	64 pins
16 KB	768 B	–	μPD78F8026	μPD78F8033
24 KB	1 KB	–	μPD78F8027	μPD78F8034
32 KB	1 KB	–	μPD78F8028	μPD78F8035
48 KB	1 KB	1 KB	μPD78F8029	μPD78F8036
60 KB	1 KB	2 KB	μPD78F8030	μPD78F8037
128 KB	1 KB	6 KB	μPD78F8032D	μPD78F8039D

Note The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

○ On-chip single-power-supply flash memory
○ Self-programming (with boot swap function)
○ On-chip debug function (μPD78F8032D and 78F8039D only[Note 1])
○ On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
○ On-chip watchdog timer (operable with the on-chip internal low speed oscillation clock)
○ On-chip multiplier/divider (16 bits x 16 bits, 32 bits x 16 bits)
○ On-chip key interrupt function
○ I/O ports: 48 pins: 23 (N-ch open drain: 2)
64 pins: 41 (N-ch open drain: 4)
○ Timer: 7 channels
- 16-bit timer/event counters: 1 channel
- 8-bit timer/event counters: 2 channels
- 8-bit timer: 2 channels
- Watch timer[Note 2]: 1 channel
- Watch dog timer: 1 channel

Notes 1. The μPD78F8032D and 78F8039D have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. μPD78F8033 to 78F8037, 78F8039D only

- Serial interface: 3 channels
  - UART (LIN (Local Interconnect Network)-bus supported): 1 channel
  - CSI/UART[Note]: 1 channel
  - IIC: 1 channel
- 10-bit resolution A/D converter: μPD78F8026 to 78F8030, 78F8032D: 4 channels
  μPD78F8033 to 78F8037, 78F8039D: 8 channels
- On-chip power supply circuit
  Output voltage: 5 V ± 2%
  On-chip over current protection circuit
  On-chip thermal shutdown circuit
- LIN transceiver

<R> The LIN transceiver complies with LIN Specifications Rev.2.0, 2.1
Low power consumption achieved with on-chip sleep function
On-chip pull-up resistor for slave applications
On-chip LIN driver over current protection circuit
On-chip LIN driver thermal shutdown circuit

- Driver
  High side driver: 1 channel
- High voltage switch input function: 1 channel

<R> - Package: 48-pin plastic LQFP (fine-pitch) (7×7)
64-pin plastic LQFP (fine-pitch) (10×10)

<R> - Operation ambient temperature: (A) grade products T_A = –40 to +85 °C

Note Select either of the functions of these alternate-function pins.

1.2 Applications

○ Automotive equipment

System control for body electronic control units

- Power windows
- Keyless entry reception
- Immobilizer
- Mirror control, etc.

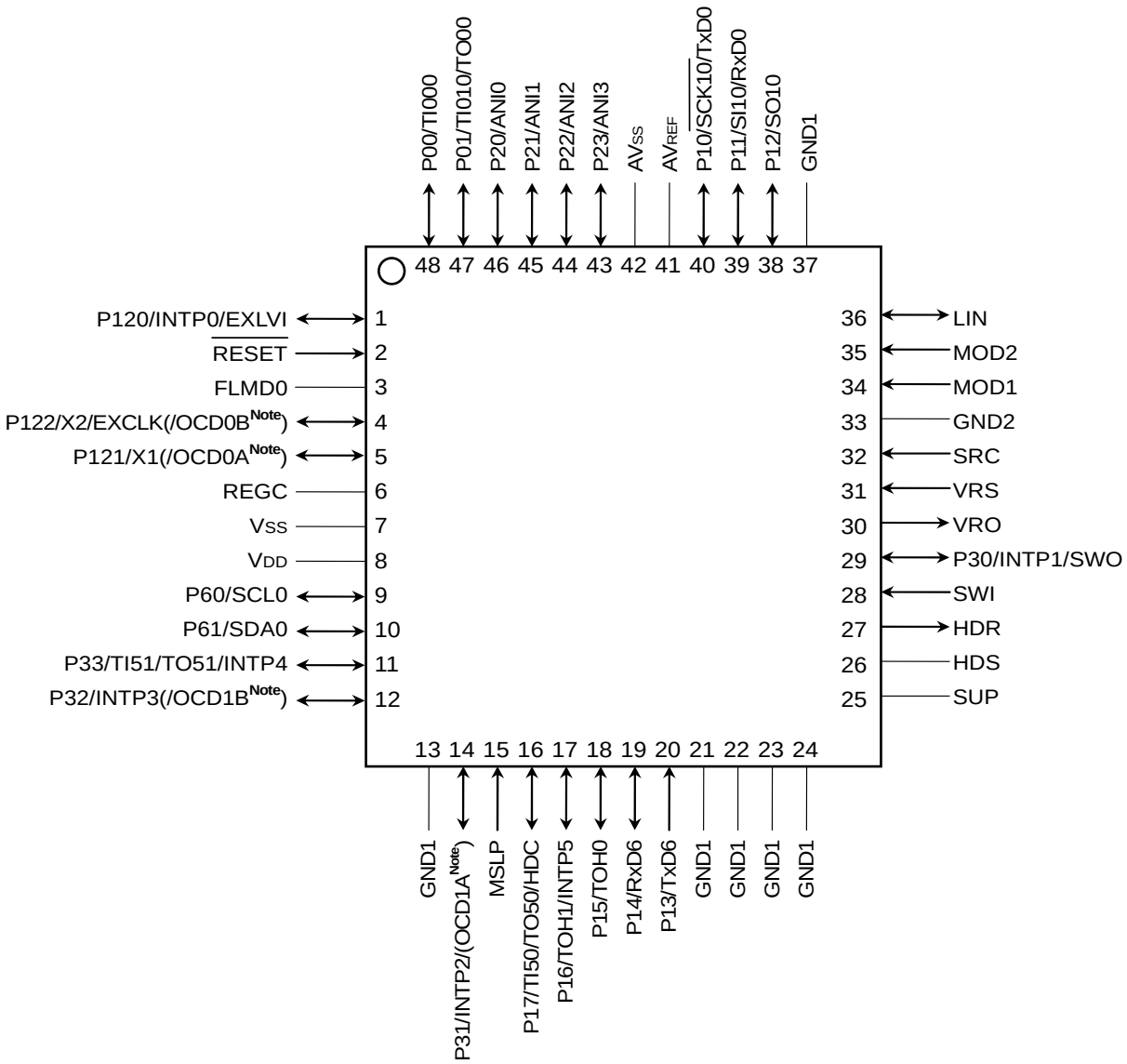
<R> 1.3 Ordering Information

Part Number	Package	Quality Grade
μPD78F8026GAA-GAM-G Note	48-pin plastic LQFP (fine pitch) (7×7)	Special
μ PD78F8027GAA-GAM-G Note	48-pin plastic LQFP (fine pitch) (7×7)	Special
μ PD78F8028GAA-GAM-G Note	48-pin plastic LQFP (fine pitch) (7×7)	Special
μ PD78F8029GAA-GAM-G Note	48-pin plastic LQFP (fine pitch) (7×7)	Special
μ PD78F8030GAA-GAM-G Note	48-pin plastic LQFP (fine pitch) (7×7)	Special
μ PD78F8032DGA-GAM-G	48-pin plastic LQFP (fine pitch) (7×7)	Standard
μ PD78F8033GBA-GAH-G Note	64-pin plastic LQFP (fine pitch) (10×10)	Special
μ PD78F8034GBA-GAH-G Note	64-pin plastic LQFP (fine pitch) (10×10)	Special
μ PD78F8035GBA-GAH-G Note	64-pin plastic LQFP (fine pitch) (10×10)	Special
μ PD78F8036GBA-GAH-G Note	64-pin plastic LQFP (fine pitch) (10×10)	Special
μ PD78F8037GBA-GAH-G Note	64-pin plastic LQFP (fine pitch) (10×10)	Special
μ PD78F8039DGB-GAH-G	64-pin plastic LQFP (fine pitch) (10×10)	Standard

Note (A) grade products

1.4 Pin Configuration (Top View)

<R> • 48-pin plastic LQFP (fine-pitch) (7×7)



Note μPD78F8032D (products with on-chip debug function) only

<R> **Cautions 1. Make GND1, GND2, AVSS, and VSS the same potential.**

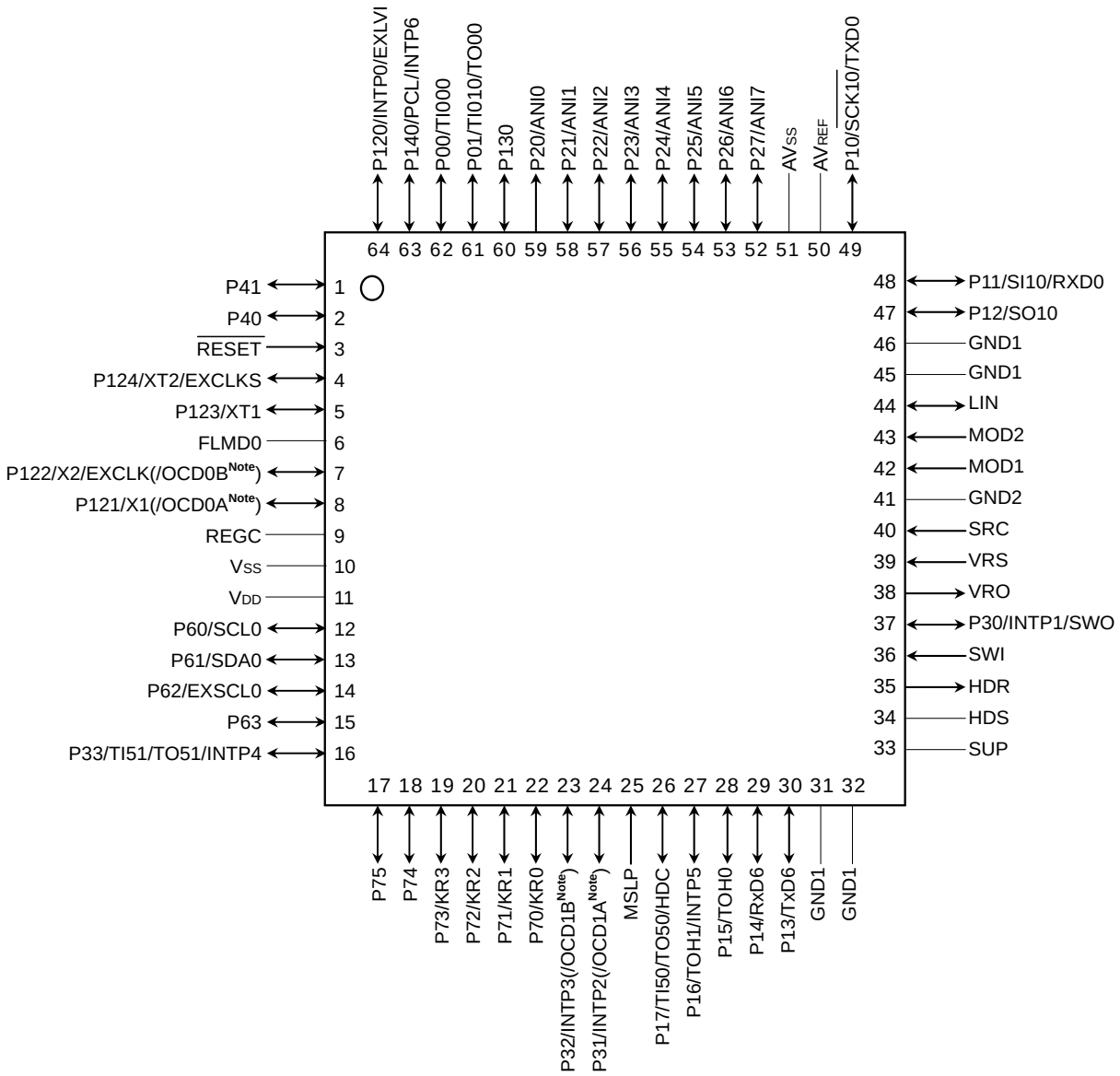
<R> **2. Connect the REGC pin to VSS via a capacitor (0.47 μF to 1 μF).**

3. ANI0/P20 to ANI3/P23 are in the analog input mode after reset release.

4. Make SUP and HDS the same potential.

<R> **5. Make VRO, VRS, and VDD the same potential.**

- 64-pin plastic LQFP (fine-pitch) (10×10)



Note μPD78F8039D (products with on-chip debug function) only

<R> **Cautions 1. Make GND1, GND2, AVSS, and VSS the same potential.**

<R> **2. Connect the REGC pin to VSS via a capacitor (0.47 μF to 1 μF).**

3. ANI0/P20 to ANI7/P27 are in the analog input mode after reset release.

4. Make SUP and HDS the same potential.

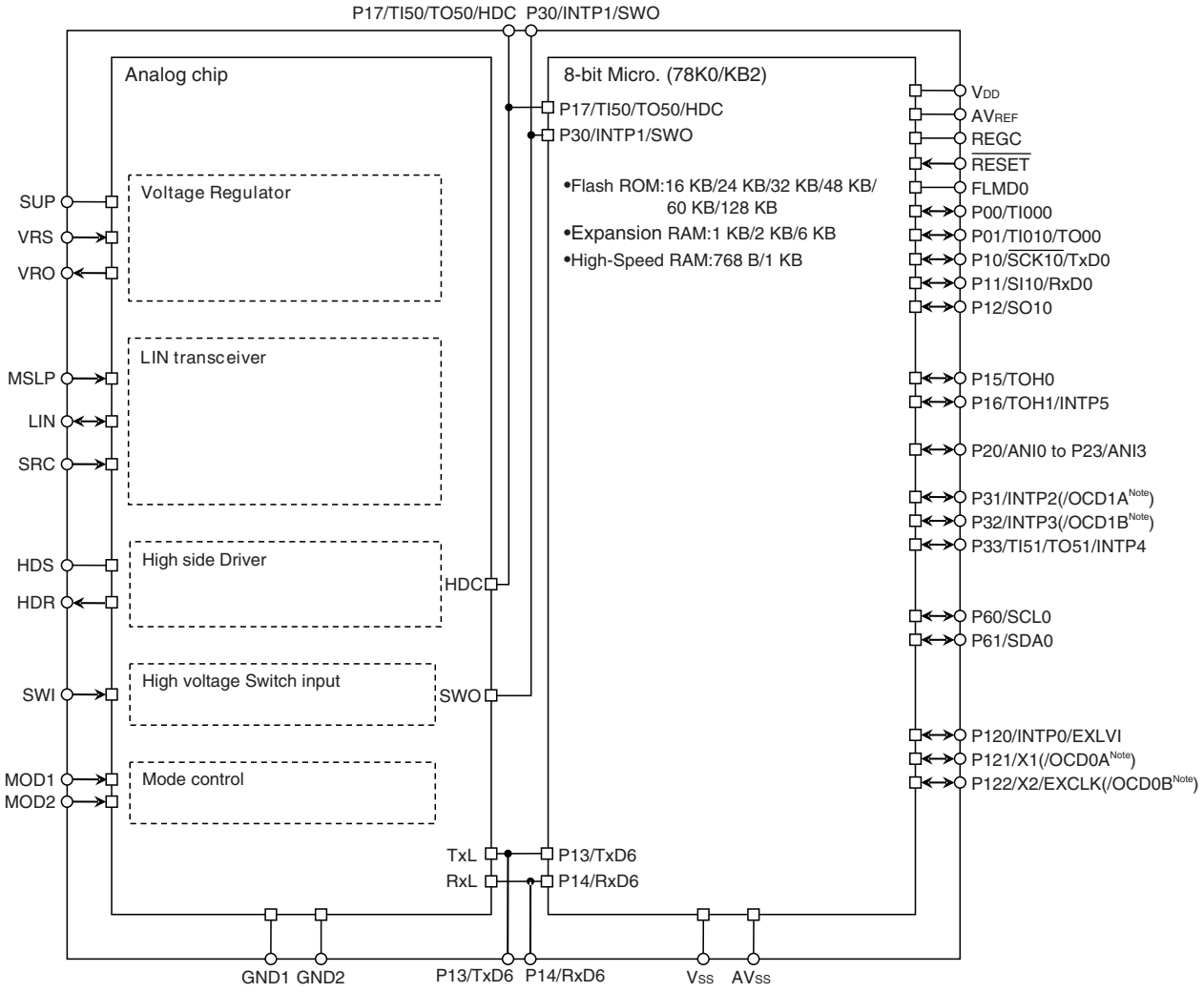
<R> **5. Make VRO, VRS, and VDD the same potential.**

Pin Identification

ANI0 to ANI7:	Analog Input	P70 to P75:	Port 7
AV_{REF}:	Analog Reference Voltage	P120 to P124:	Port 12
AV_{SS}:	Analog Ground	P130:	Port 13
EXCLK:	External Clock Input (Main System Clock)	P140:	Port 14
		PCL:	Programmable Ckock Output
EXCLKS:	External Clock Input (Subsystem Clock)	REGC:	Regulator Capacitance
		$\overline{\text{RESET}}$:	Reset
EXLVI:	External potential Input for Low-voltage detector	RxD0, RxD6:	Receive Data
		$\overline{\text{SCK10}}$, SCL0:	Serial Clock Input/Output
EXSCL0:	IIC0 Serial Clock Input/Output	SDA0:	Serial Data Input/Output
FLMD0:	Flash Programming Mode	SI10:	Serial Data Input
GND1, GND2:	Ground	SO10:	Serial Data Output
HDC:	High-side Driver Control Input	SRC:	Slew Rate Contorol Input
HDR:	High-side Driver Output	SUP:	Battery Power Supply
HDS:	High-side Driver Power Supply	SWI:	High Voltage SW Input
INTP0 to INTP6:	External Interrupt Input	SWO:	High Voltage SW Output
KR0 to KR3:	Key Return	TI000 TI010,	
LIN:	LIN Bus	TI50, TI51:	Timer Input
MOD1, MOD2:	Pin Mode Control Input	TO00, TO01,	
MSLP:	Sleep Mode Control Input	TO50, TO51,	
OCD0A, OCD0B,		TOH0, TOH1:	Timer Output
OCD1A, OCD1B:	On-Chip Debug Input/Output	TxD0, TxD6:	Transmit Data
P00, P01:	Port 0	V_{DD}:	Power Supply
P10 to P17:	Port 1	VRO:	Voltage Regulator Output
P20 to P27:	Port 2	VRS:	Voltage Regulator Input
P30 to P33:	Port 3	V_{SS}:	Ground
P40, P41:	Port 4	X1, X2:	Crystal Oscillator (Main System Clock)
P60 to P63:	Port 6	XT1, XT2:	Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

• μPD78F8026 to 78F8030, 78F8032D

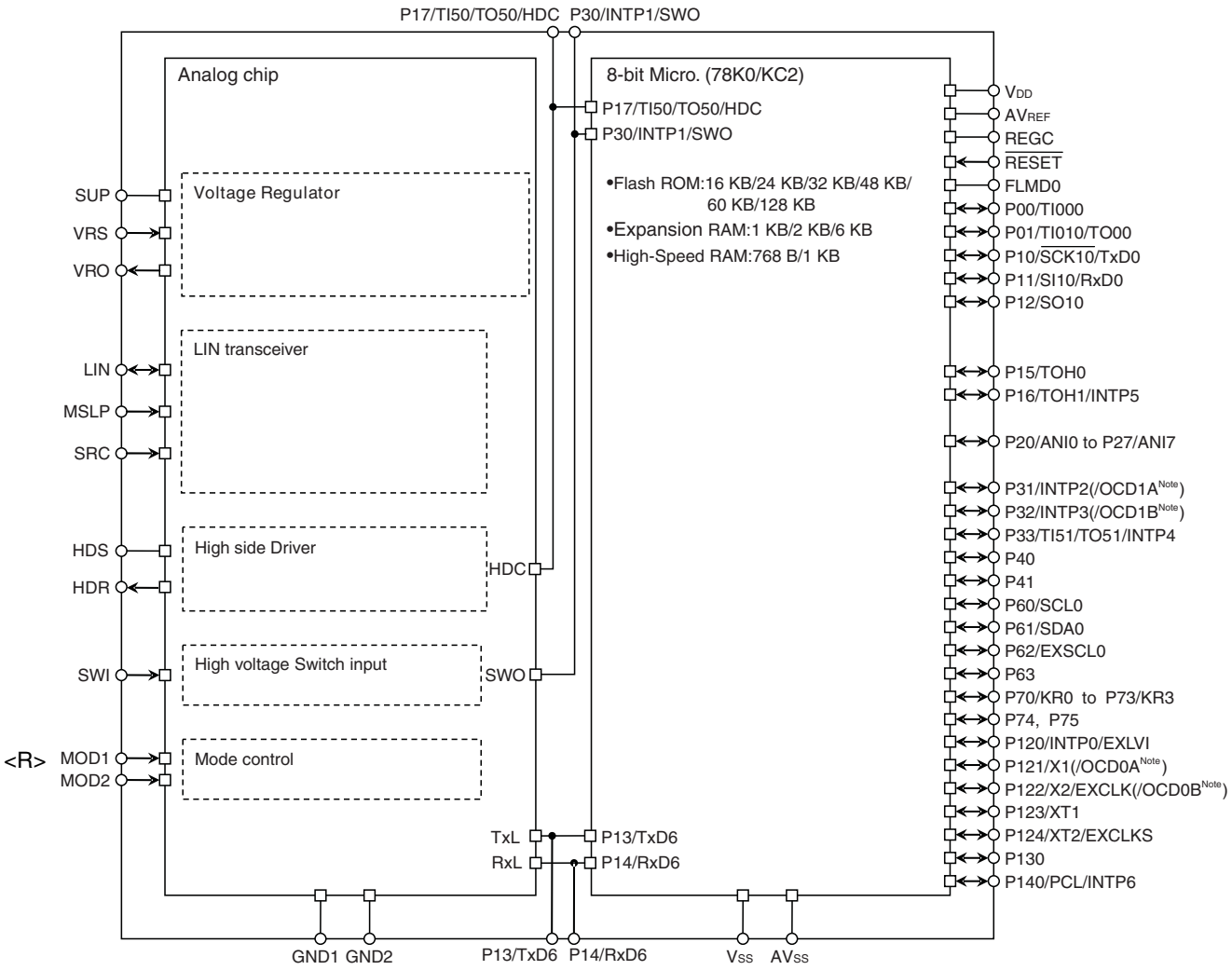


Note μPD78F8032D (products with on-chip debug function) only

Cautions 1. μPD78F8026 to 78F8030, and 78F8032D are developed as MCP (Multi-Chip Package) which includes 2 chips in the package, a microcontroller and an analog chip (power supply circuit and LIN transceiver).

2. The P13/TxD6, P14/RxD6, P17/TI50/TO50/HDC and P30/INTP1/SWO terminals are connected with the analog block inside the package.

• μPD78F8033 to 78F8037, 78F8039D



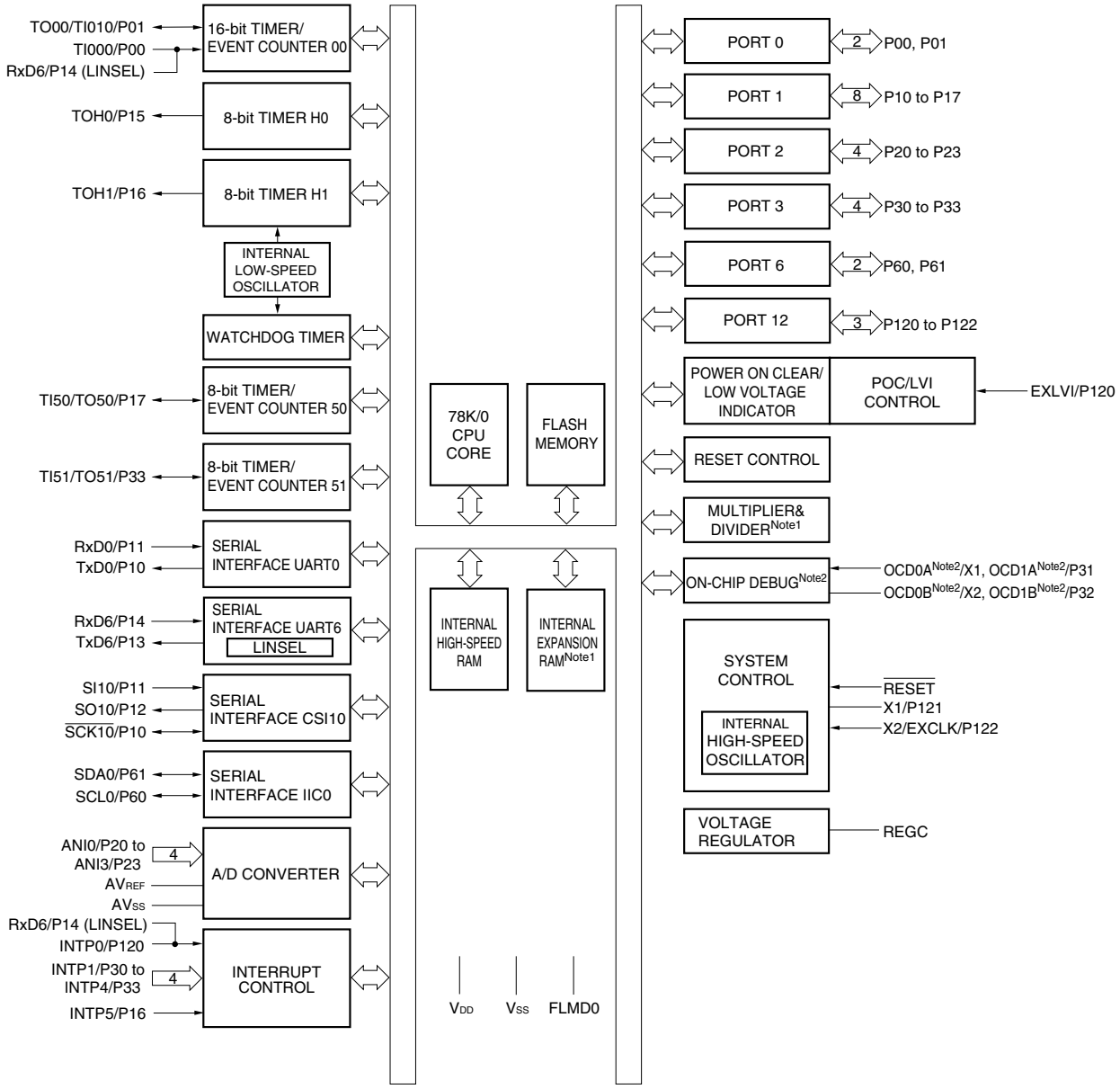
Note μPD78F8039D (products with on-chip debug function) only

Cautions 1. μPD78F8033 to 78F8037, and 78F8039D are developed as MCP (Multi-Chip Package) which includes 2 chips in the package, a microcontroller and an analog chip (power supply circuit and LIN transceiver).

2. The P13/TxD6, P14/RxD6, P17/TI50/TO50/HDC and P30/INTP1/SWO terminals are connected with the analog block inside the package.

1.5.1 Microcontroller block diagram

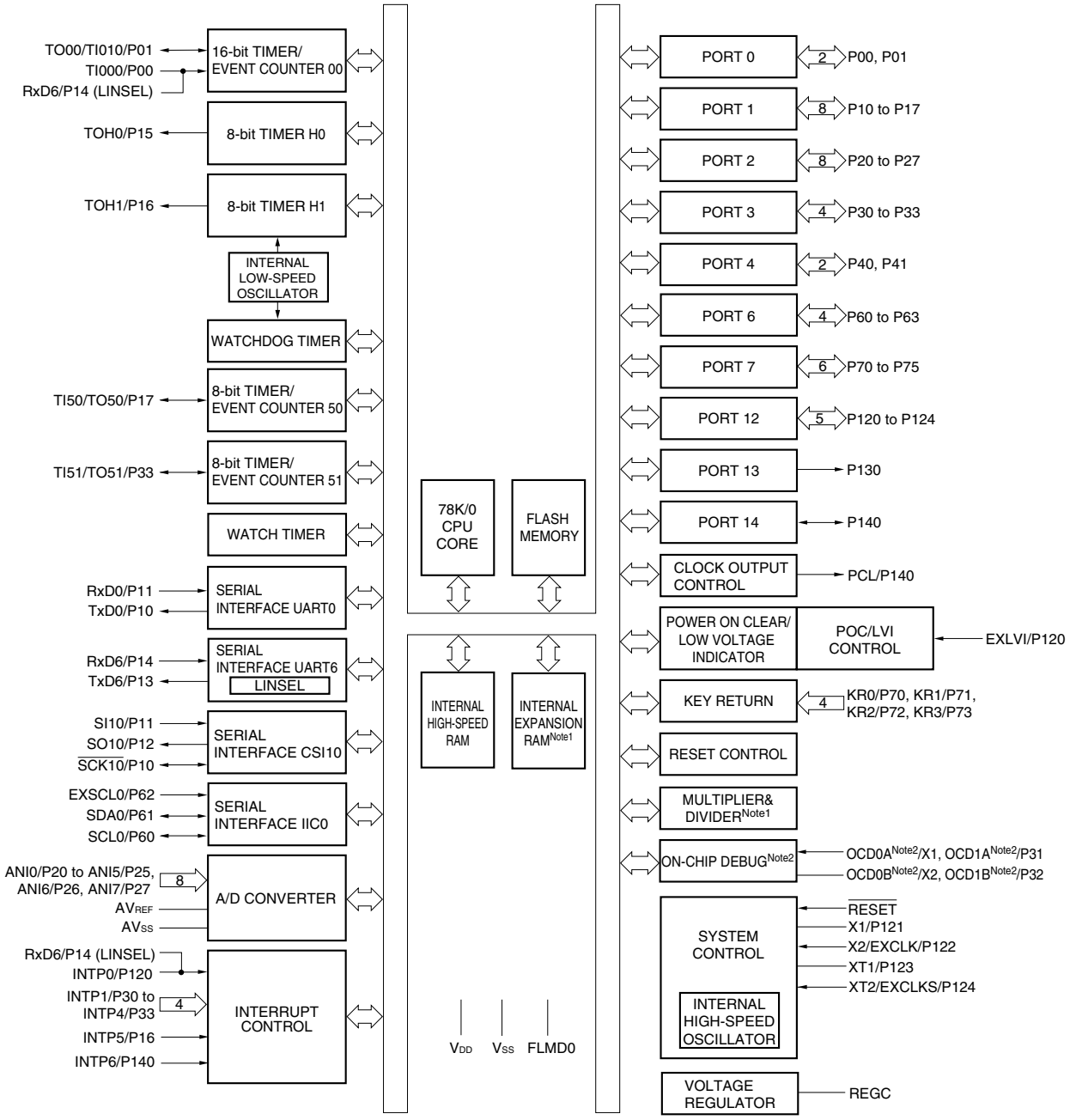
• μPD78F8026 to 78F8030, 78F8032D



Notes 1. μPD78F8029, 78F8030, and 78F8032D only

2. μPD78F8032D only

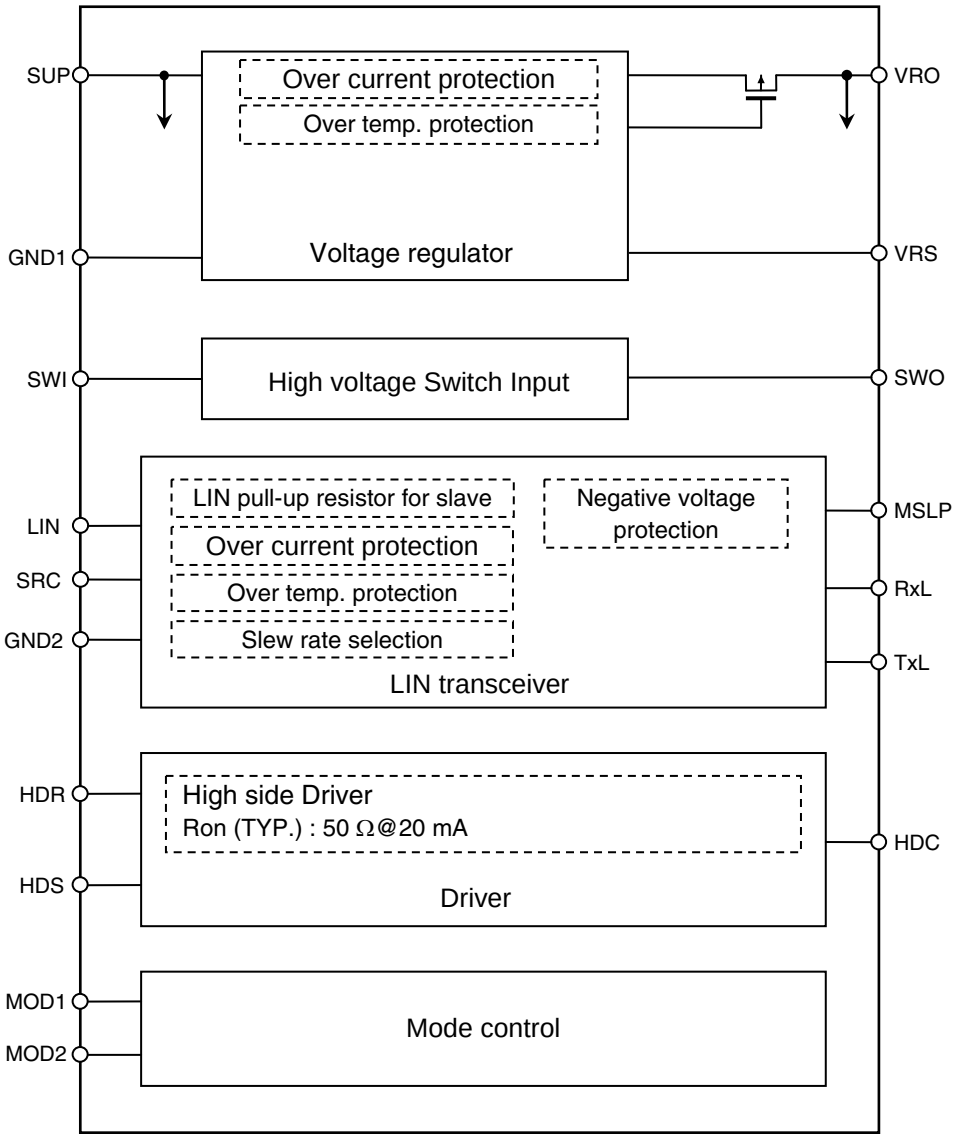
• μPD78F8033 to 78F8037, 78F8039D



Notes 1. μPD78F8036, 78F8037, and 78F8039D only

2. μPD78F8039D only

1.5.2 Analog block diagram



1.6 Outline of Functions

• μPD78F8026 to 78F8030, 78F8032D

(1/2)

	Item		μPD78F8026	μPD78F8027	μPD78F8028	μPD78F8029	μPD78F8030	μPD78F8032D
	Flash memory (KB)		16	24	32	48	60	128
	High-Speed RAM		768 Bytes	1 KB				
	Expansion RAM (KB)		–			1	2	6
	Bank (flash memory)		–					6
<R>	Power supply voltage		(A) grade products: V_{DD} = 1.8 to 5.5 V					
	Regulator		Provided					
	Minimum instruction execution time		0.1 μs (20 MHz: V_{DD} = 2.7 to 5.5 V)/0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)					
Clock	Main	High-speed system	20 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V					
		Internal high-speed oscillation	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V					
	Subsystem		–					
	Internal low-speed oscillation		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V					
Port	Total		23					
	N-ch O.D. (6 V tolerance)		2					
Timer	16 bits (TM0)		1 ch					
	8 bits (TM5)		2 ch					
	8 bits (TMH)		2 ch					
	Watch		–					
	WDT		1 ch					
Serial interface	UART/3-wire CSI Note 1		1 ch					
	UART supporting LIN-bus		1 ch					
	I^2C bus		1 ch					
	10-bit A/D		4 ch					
Interrupt	External		6					
	Internal		14					
	Key interrupt		–					
Reset	$\overline{\text{RESET}}$ pin		Provided					
	POC		1.59 V ±0.15 V					
	LVI		The detection level of the supply voltage is selectable.					
	WDT		Provided					
	Multiplier/divider		–			Provided		
	On-chip debug function		–					Provided
<R>	Operating ambient temperature		T_A = –40 to +85°C					

Note Select either of the functions of these alternate-function pins.

(2/2)

Item	μPD78F8026	μPD78F8027	μPD78F8028	μPD78F8029	μPD78F8030	μPD78F8032D
Power Supply	• Operating supply voltage range: 6 V to 19 V (output voltage: 5 V±5%, output current: 25 mA Max.) 7 V to 19 V (output voltage: 5 V±5%, output current: 50 mA Max.) • Include P-ch MOS for dropper • Output voltage: 5 V ± 2% • On-chip over current protection circuit • On-chip thermal shutdown circuit					
<R> LIN transceiver	• The LIN transceiver complies with LIN Specifications Rev.2.0, 2.1 • Low power consumption achieved with on-chip sleep function • On-chip Slew rate select function • On-chip pull-up resistors for slave applications • On-chip LIN driver current protection circuit • On-chip LIN driver thermal shutdown circuit					
Driver	• High side driver: 1 channel					
High voltage switch input function	1 channel					

An outline of the timer is shown below.

		16-Bit Timer/ Event Counters 00 and 01		8-Bit Timer/ Event Counters 50 and 51		8-Bit Timers H0 and H1		Watch Timer	Watchdog Timer
		TM00	TM01	TM50	TM51	TMH0	TMH1		
Function	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel	–	–
	External event counter	1 channel	1 channel	1 channel	1 channel	–	–	–	–
	PPG output	1 output	1 output	–	–	–	–	–	–
	PWM output	–	–	1 output	1 output	1 output	1 output	–	–
	Pulse width measurement	2 inputs	2 inputs	–	–	–	–	–	–
	Square-wave output	1 output	1 output	1 output	1 output	1 output	1 output	–	–
	Carrier generator	–	–	–	–	–	1 output[Note]	–	–
	Watch Timer	–	–	–	–	–	–	–	–
	Watchdog timer	–	–	–	–	–	–	–	1 channel
Interrupt source		2	2	1	1	1	1	–	–

Note TM51 and TMH1 can be used in combination as a carrier generator mode.

• μPD78F8033 to 78F8037, 78F8039D

(1/2)

Item			μPD78F8033	μPD78F8034	μPD78F8035	μPD78F8036	μPD78F8037	μPD78F8039D
Flash memory (KB)			16	24	32	48	60	128
High-Speed RAM			768 Bytes	1 KB				
Expansion RAM (KB)			–			1	2	6
Bank (flash memory)			–					6
Power supply voltage			(A) grade products: V_{DD} = 1.8 to 5.5 V					
Regulator			Provided					
Minimum instruction execution time			0.1 μs (20 MHz: V_{DD} = 2.7 to 5.5 V)/0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)					
Clock	Main	High-speed system	20 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V					
		Internal high-speed oscillation	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V					
	Subsystem		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V					
	Internal low-speed oscillation		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V					
Port	Total		41					
	N-ch O.D. (6 V tolerance)		4					
Timer	16 bits (TM0)		1 ch					
	8 bits (TM5)		2 ch					
	8 bits (TMH)		2 ch					
	Watch		1 ch					
	WDT		1 ch					
Serial interface	UART/3-wire CSI Note		1 ch					
	UART supporting LIN-bus		1 ch					
	I^2C bus		1 ch					
10-bit A/D			8 ch					
Interrupt	External		8					
	Internal		16					
Key interrupt			4 ch					
Reset	$\overline{\text{RESET}}$ pin		Provided					
	POC		1.59 V ±0.15 V					
	LVI		The detection level of the supply voltage is selectable.					
	WDT		Provided					
Multiplier/divider			–			Provided		
On-chip debug function			–					Provided
Operating ambient temperature			T_A = –40 to +85°C					

Note Select either of the functions of these alternate-function pins.

(2/2)

Item	μPD78F8033	μPD78F8034	μPD78F8035	μPD78F8036	μPD78F8037	μPD78F8039D
Power Supply	• Input voltage: V_{SUP} = 6 V to 19 V • Include P-ch MOS for dropper • Output voltage: 5 V ± 2% • On-chip over current protection circuit • On-chip thermal shutdown circuit					
<R> LIN transceiver	• The LIN transceiver complies with LIN Specifications Rev.2.0, 2.1 • Low power consumption achieved with on-chip sleep function • On-chip Slew rate select function • On-chip pull-up resistors for slave applications • On-chip LIN driver current protection circuit • On-chip LIN driver thermal shutdown circuit					
Driver	• High side driver: 1 channel					
High voltage switch input function	1 channel					

An outline of the timer is shown below.

		16-Bit Timer/ Event Counters 00 and 01		8-Bit Timer/ Event Counters 50 and 51		8-Bit Timers H0 and H1		Watch Timer	Watchdog Timer
		TM00	TM01	TM50	TM51	TMH0	TMH1		
Function	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel Note 1	–
	External event counter	1 channel	1 channel	1 channel	1 channel	–	–	–	–
	PPG output	1 output	1 output	–	–	–	–	–	–
	PWM output	–	–	1 output	1 output	1 output	1 output	–	–
	Pulse width measurement	2 inputs	2 inputs	–	–	–	–	–	–
	Square-wave output	1 output	1 output	1 output	1 output	1 output	1 output	–	–
	Carrier generator	–	–	–	–	–	1 output Note 2	–	–
	Watch Timer	–	–	–	–	–	–	1 channel Note 1	–
	Watchdog timer	–	–	–	–	–	–	–	1 channel
Interrupt source		2	2	1	1	1	1	1	–

Notes 1. In the watch timer, the watch timer function and interval timer function can be used simultaneously.

2. TM51 and TMH1 can be used in combination as a carrier generator mode.

CHAPTER 2 PIN FUNCTIONS

2.1 μPD78F8026 to 78F8030, 78F8032D

The following microcontroller function pins differ between the μPD78F8026 to 78F8030, 78F8032D, and 78K0/KB2.

(1) Port and alternate function pins

μPD78F8026, 78F8027, 78F8028, 78F8029, 78F8030, 78F8032D		78K0/KB2 μPD78F0500A, 78F0501A, 78F05302A, 78F0503A, 78F0504A, 78F0505A, 78F0507DA	
Pin name	Alternate function	Pin name	Alternate function
P17	TI50/TO50/HDC	P17	TI50/TO50
P30	INTP1/SWO	P30	INTP1

2.2 μPD78F8033 to 78F8037, 78F8039D

The following microcontroller function pins differ between the μPD78F8033 to 78F8037, 78F8039D, and 78K0/KC2.

(1) Port and alternate function pins

μPD78F8033, 78F8034, 78F8035, 78F8036, 78F8037, 78F8039D		78K0/KC2 μPD78F0510A, 78F0511A, 78F05312A, 78F0513A, 78F0514A, 78F0515A, 78F0517DA	
Pin name	Alternate function	Pin name	Alternate function
P17	TI50/TO50/HDC	P17	TI50/TO50
P30	INTP1/SWO	P30	INTP1

2.3 Microcontroller Part Pin Functions

There are two types of pin I/O buffer power supplies: AV_{REF}, and V_{DD}. The relationship between these power supplies and the pins are shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27
V_{DD}	Pins other than P20 to P27

2.3.1 μPD78F8026 to 78F8030, 78F8032D

(1) Port Functions : μPD78F8026 to 78F8030, 78F8032D

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK10}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50/HDC[Note 1]
P20 to P23	I/O	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI3
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/SWO[Note 2]
P31				INTP2/OCD1A[Note 3]
P32				INTP3/OCD1B[Note 3]
P33				TI51/TO51/INTP4
P60	I/O	Port 6. 2-bit I/O port. Output of P60 to P61 is N-ch open-drain output (6V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P120	I/O	Port 12. 3-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1/OCD0A[Note 3]
P122				X2/EXCLK/OCD0B[Note 3]

Notes 1. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the HDC pin in the package analog block.

2. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the SWO pin in the package analog block.

3. μPD78F8032D only

(2) Non-port functions (1/2) : μPD78F8026 to 78F8030, 78F8032D

	Function Name	I/O	Function	After Reset	Alternate Function
	INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
	INTP1				P30/SWO[Note 1]
	INTP2				P31/OCD1A[Note 2]
	INTP3				P32/OCD1B[Note 2]
	INTP4				P33/TI51/TO51
	INTP5				P16/TOH1
<R>	SI10	Input	Serial data input to CSI10	Input port	P11/RxD0
<R>	SO10	Output	Serial data output from CSI10	Input port	P12
<R>	SDA0	I/O	Serial data I/O for I^2C	Input port	P61
<R>	$\overline{SCK10}$	I/O	Clock input/output for CSI10	Input port	P10/TxD0
<R>	SCL0		Clock input/output for I^2C		P60
<R>	RxD0	Input	Serial data input to UART0	Input port	P11/SI10
<R>	RxD6		Serial data input to UART6		P14
<R>	TxD0	Output	Serial data output from UART0	Input port	P10/$\overline{SCK10}$
<R>	TxD6		Serial data output from UART6		P13
	TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
	TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
	TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
	TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50/HDC[Note 3]
	TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
	TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50/HDC[Note 3]
	TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
	TOH0		8-bit timer H0 output		P15
	TOH1		8-bit timer H1 output		P16/INTP5
	ANI0 to ANI3	Input	A/D converter analog input	Analog input	P20 to P23
<R>	AV_{REF}	–	A/D converter reference voltage input and positive power supply for P20 to P23 and A/D converter	–	–
	AV_{SS}	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–
<R>	REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 μF to 1 μF).	–	–
	$\overline{RESET}$	Input	System reset input	–	–
	EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0

Notes 1. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the SWO pin in the package analog block.

2. μPD78F8032D only

3. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the HDC pin in the package analog block.

(2) Non-port functions (2/2) : μPD78F8026 to 78F8030, 78F8032D

	Function Name	I/O	Function	After Reset	Alternate Function
<R>	X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A[Note]
	X2	–			P122/EXCLK/ OCD0B[Note]
	EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B Note
<R>	V_{DD}	–	Positive power supply for pins other than P20 to P23	–	–
<R>	V_{SS}	–	Ground potential for pins other than P20 to P23	–	–
	FLMD0	–	Flash memory programming mode setting	–	–
	OCD0A[Note]	Input	Connection for on-chip debug mode setting pins (μPD78F8032D only)	Input port	P121/X1
	OCD1A[Note]				P31/INTP2
	OCD0B[Note]	–			P122/X2/EXCLK
	OCD1B[Note]				P32/INTP3

Note μPD78F8032D only

2.3.2 μPD78F8033 to 78F8037, 78F8039D

(1) Port functions (1/2) : μPD78F8033 to 78F8037, 78F8039D

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK10}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50/HDC[Note 1]
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI7
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/SWO[Note 2]
P31				INTP2/OCD1A[Note 3]
P32				INTP3/OCD1B[Note 3]
P33				TI51/TO51/INTP4

Notes 1. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the HDC pin in the package analog block.

2. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the SWO pin in the package analog block.

3. μPD78F8039D only

(1) Port functions (2/2) : μPD78F8033 to 78F8037, 78F8039D

Function Name	I/O	Function	After Reset	Alternate Function
P40, P41	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input	–
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P61 is N-ch open-drain output (6V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P62				EXSCL0
P63				–
P70 to P73	I/O	Port 7. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR3
P74, P75				–
P120	I/O	Port 12. 5-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1/OCD0A Note
P122				X2/EXCLK/OCD0B Note
P123				XT1 Note
P124				XT2/EXCLKS Note
P130	Output	Port 13. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P140	I/O	Port 14. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCL/INTP6

Note μPD78F8039D only

(2) Non-port functions (1/3) : μPD78F8033 to 78F8037, 78F8039D

Function Name	I/O	Function	After Reset	Alternate Function
EXSCL0	Input	External clock input for I^2C. To input an external clock, input a clock of 6.4 MHz.	Input port	P62
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30/SWO Note 1
INTP2				P31/OCD1A Note 2
INTP3				P32/OCD1B Note 2
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
INTP6				P140/PCL
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73

Notes 1. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the SWO pin in the package analog block.

2. μPD78F8039D only

(2) Non-port functions (2/3) : μPD78F8033 to 78F8037, 78F8039D

	Function Name	I/O	Function	After Reset	Alternate Function
	PCL	Output	Clock output (for trimming of high-speed system clock, subsystem clock)	Input port	P140/INTP6
<R>	SI10	Input	Serial data input to CSI10	Input port	P11/RxD0
<R>	SO10	Output	Serial data output from CSI10	Input port	P12
<R>	SDA0	I/O	Serial data I/O for I^2C	Input port	P61
<R>	$\overline{SCK10}$	I/O	Clock input/output for CSI10	Input port	P10/TxD0
<R>	SCL0		Clock input/output for I^2C		P60
<R>	RxD0	Input	Serial data input to UART0	Input port	P11/SI10
<R>	RxD6		Serial data input to UART6		P14
<R>	TxD0	Output	Serial data output from UART0	Input port	P10/$\overline{SCK10}$
<R>	TxD6		Serial data output from UART6		P13
	TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
	TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
	TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
	TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50/HDC[Note 1]
	TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
	TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50/HDC[Note 1]
	TOH0		8-bit timer H0 output		P15
	TOH1		8-bit timer H1 output		P16/INTP5
	ANI0 to ANI7	Input	A/D converter analog input	Analog input	P20 to P27
<R>	AV_{REF}	–	A/D converter reference voltage input and positive power supply for P20 to P23 and A/D converter	–	–
	AV_{SS}	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–
<R>	REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 μF to 1 μF).	–	–
	$\overline{RESET}$	Input	System reset input	–	–
	EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
<R>	X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A[Note 2]
	X2	–			P122/EXCLK/OCD0B[Note 2]
	EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B[Note 2]
<R>	XT1	–	Connecting resonator for subsystem clock	Input port	P123
	XT2	–			P122/EXCLKS
	EXCLKS	Input	External clock input for subsystem clock	Input port	P122/XT2

Notes 1. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the HDC pin in the package analog block.

2. μPD78F8039D only

(2) Non-port functions (3/3) : μPD78F8033 to 78F8037, 78F8039D

Function Name	I/O	Function	After Reset	Alternate Function
<R> V_{DD}	–	Positive power supply for pins other than P20 to P27	–	–
<R> V_{SS}	–	Ground potential for pins other than P20 to P27	–	–
FLMD0	–	Flash memory programming mode setting	–	–
OCD0A[Note]	Input	Connection for on-chip debug mode setting pins (μPD78F8039D only)	Input port	P121/X1
OCD1A[Note]				P31/INTP2
OCD0B[Note]	–			P122/X2/EXCLK
OCD1B[Note]				P32/INTP3

Note μPD78F8039D only

2.4 Analog Part Pins

Function Name	I/O	Function
GND1	–	Power supply circuit GND
GND2	–	LIN transceiver circuit GND
HDC Note 1	Input	High side driver control input
HDR	Output	High side driver control output
HDS	–	High side driver power supply
LIN	I/O	LIN Bus connection pin
MOD1, MOD2	Input	Pin mode control input
MSLP	Input	Sleep mode select
SRC	Input	Slew rate control input
SUP	–	Power supply connection pin
SWI	Input	High voltage switch input
SWO Note 2	Output	High voltage switch output
VRO	Output	Supply voltage output
VRS	Input	Power supply/voltage regulator monitor

Notes 1. The pins to which these functions are assigned are connected to the P17/TI50/TO50 pin in the package microcontroller block.

2. The pins to which these functions are assigned are connected to the P30/INTP1 pin in the package microcontroller block.

Cautions 1. Make GND1, GND2 the same potential as V_{SS} and AV_{SS}

2. Make SUP the same potential as HDS.

3. Make VRO the same potential as VRO, VRS.

2.5 Description of Pin Functions

Remark The pins mounted depend on the product. See **1.3 Ordering Information** and **2.3 Microcontroller Part Pin Functions**.

2.5.1 P00, P01 (port 0)

2-bit I/O port. These pins also function as timer I/O.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P00/TI000	√	
P01/TI010/TO00	√	

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

2-bit I/O port. P00, P01can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00, P01 function as timer I/O.

(a) TI000

These are the pins for inputting an external count clock to 16-bit timer/event counters 00 and are also for inputting a capture trigger signal to the capture registers (CR000, CR010) of 16-bit timer/event counters 00.

(b) TI010

These are the pins for inputting a capture trigger signal to the capture register (CR000) of 16-bit timer/event counters 00.

(c) TO00

These are timer output pins of 16-bit timer/event counters 00.

2.5.2 P10 to P17 (port 1)

P10 to P17 function as an 8-bit I/O port. These pins also function as pins for external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P10/$\overline{\text{SCK10}}$/TxD0	√	
P11/SI10/RxD0	√	
P12/SO10	√	
P13/TxD6	√	
P14/RxD6	√	
P15/TOH0	√	
P16/TOH1/INTP5	√	
P17/TI50/TO50/HDC[Note]	√	

Note These are the functions of the analog pins. The pins to which these functions are assigned are connected to the HDC pin in the package analog block.

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an 8-bit I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

(a) SI10

This is a serial data input pin of serial interface CSI10.

(b) SO10

This is a serial data output pin of serial interface CSI10.

(c) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(d) RxD0

This is a serial data input pin of serial interface UART0.

(e) RxD6

This is a serial data input pin of serial interface UART6.

(f) TxD0

This is a serial data output pin of serial interface UART0.

(g) TxD6

This is a serial data output pin of serial interface UART6.

(h) TI50

This is the pin for inputting an external count clock to 8-bit timer/event counter 50.

(i) TO50

This is a timer output pin of 8-bit timer/event counter 50.

(j) TOH0, TOH1

These are the timer output pins of 8-bit timers H0 and H1.

(k) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.5.3 P20 to P27 (port 2)

P20 to P27 function as an 8-bit I/O port. These pins also function as pins for A/D converter analog input.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P20/ANI0	√	√
P21/ANI1	√	√
P22/ANI2	√	√
P23/ANI3	√	√
P24/ANI4	–	√
P25/ANI5	–	√
P26/ANI6	–	√
P27/ANI7	–	√

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an 8-bit I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as A/D converter analog input pins (ANI0 to ANI7). When using these pins as analog input pins, see **13.6 Cautions for A/D Converter in 78K0/Kx2 User's Manual (R01UH0008E)**.

(a) ANI0 to ANI7

These are A/D converter analog input pins.

Caution ANI0/P20 to ANI7/P27 are set to analog input mode after reset release.

2.5.4 P30 to P33 (port 3)

P30 to P33 function as a 4-bit I/O port. These pins also function as pins for external interrupt request input and timer I/O.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P30/INTP0/SWO[Note 1]	√	
P31/INTP1/OCD1A[Note 2]	√	
P32/INTP2/OCD1B[Note 2]	√	
P33/INTP3/TI51/TO51	√	

Notes 1. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the SWO pin in the package analog block.

2. OCD1A and OCD1B are provided to the products with an on-chip debug function (μPD78F8032D and 78F8039D) only.

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as a 4-bit I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as external interrupt request input and timer I/O.

(a) INTP1 to INTP4

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI51

This is an external count clock input pin to 8-bit timer/event counter 51.

(c) TO51

This is a timer output pin from 8-bit timer/event counter 51.

Caution 1. In the μPD78F8032D and 78F8039D, be sure to pull down pin P31 before reset release to prevent malfunction.

Caution 2. Process the P31/INTP2/OCD1A pin of the products mounted with the on-chip debug function (μPD78F8032D and 78F8039D) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P31/INTP2/OCD1A
Flash memory programmer connection		Connect to V_{SS}[Note] via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to V_{DD}[Note] or V_{SS}[Note] via a resistor. Output: Leave open.

Remark Only for μPD78F8032D and 78F8039D, P31 and P32 can be used as on-chip debug mode setting pins (OCD1A, OCD1B) when the on-chip debug function is used. For how to connect an in-circuit emulator supporting on-chip debugging (QB-78K0MINI), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION in 78K0/Kx2 User's Manual (R01UH0008E).**

2.5.5 P40 and P41 (port 4)

P40 and P41 function as a 2-bit I/O port. P40 and P41 can be set to input or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P40	–	√
P41	–	√

Remark √: Mounted, –: Not mounted

2.5.6 P60 to P63 (port 6)

P60 to P63 function as a 4-bit I/O port. These pins also function as pins for serial interface data I/O, clock I/O.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P60/SCL0	√	√
P61/SDA0	√	√
P62/EXSCL0	–	√
P63	–	√

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P60 to P63 function as a 4-bit I/O port. P60 to P63 can be set to input port or output port in 1-bit units using port mode register 6 (PM6).

Output of P60 to P63 is N-ch open-drain output (6 V tolerance).

(2) Control mode

P60 to P63 function as serial interface data I/O, clock I/O.

(a) SDA0

This is a serial data I/O pin for serial interface IIC0.

(b) SCL0

This is a serial clock I/O pin for serial interface IIC0.

(c) EXSCL0

This is an external clock input pin to serial interface IIC0. To input an external clock, input a clock of 6.4 MHz.

2.5.7 P70 to P75 (port 7)

P70 to P75 function as a 6-bit I/O port. These pins also function as key interrupt input pins.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P70/KR0	–	√
P71/KR1	–	√
P72/KR2	–	√
P73/KR3	–	√
P74	–	√
P75	–	√

Remark √: Mounted, –: Not mounted

The following operation modes can be specified.

(1) Port mode

P70 to P75 function as a 6-bit I/O port. P70 to P75 can be set to input or output port using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 to P75 function as key interrupt input pins.

(a) KR0 to KR3

This is a key interrupt input pins

2.5.8 P120 to P124 (port 12)

P120 to P124 function as a 5-bit I/O port. These pins also function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock connecting resonator for subsystem clock, external clock input for main system clock, and external clock input for subsystem clock.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P120/INTP0/EXLVI	√	√
P121/X1/OCD0A[Note]	√	√
P122/X2/EXCLK/ OCD0B[Note]	√	√
P123/XT1	–	√
P124/XT2/EXCLKS	–	√

Note OCD0A and OCD0B are provided to the products with an on-chip debug function (μPD78F8032D and 78F8039D) only.

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 to P124 function as a 5-bit I/O port. P120 to P124 can be set to input or output port using port mode register 12 (PM12). Only for P120, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

(2) Control mode

P120 to P124 function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, and external clock input for subsystem clock.

(a) INTP0

This functions as an external interrupt request input (INTP0) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

(e) XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

(f) EXCLKS

This is an external clock input pin for subsystem clock.

Caution Process the P121/X1/OCD0A pin of the products mounted with the on-chip debug function (μPD78F8032D and 78F8039D) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

Remark Only for μPD78F8032D and 78F0839D, X1 and X2 can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For how to connect an in-circuit emulator supporting on-chip debugging (QB-78K0MINI), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION in 78K0/Kx2 User's Manual (R01UH0008E).**

2.5.9 P130 (port 13)

P130 functions as an output-only port.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P130	–	√

Remarks 1. When the device is reset, P130 outputs a low level. Therefore, to output a high level from P130 before the device is reset, the output signal of P130 can be used as a pseudo reset signal of the CPU (see the figure for **Remark** in **5.2.10 Port 13 in 78K0/Kx2 User's Manual (R01UH0008E)**).

2. √: Mounted, –: Not mounted

2.5.10 P140 (port 14)

P140 function as an I/O port. These pins also function as external interrupt request input, clock output.

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
P140/PCL/INTP6	–	√

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P140 function as an I/O port. P140 can be set to input or output port in 1-bit units using port mode register 14 (PM14). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

(2) Control mode

P140 function as external interrupt request input, clock output.

(a) INTP6

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) PCL

This is a clock output pin.

2.5.11 AV_{REF}, AV_{SS}, V_{DD}, V_{SS}

	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
AV_{REF}	√	
AV_{SS}	√	
V_{DD}	√	
V_{SS}	√	

Remark √: Mounted

(a) AV_{REF}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P27 and A/D converter.

When the A/D converter is not used, connect this pin directly to V_{DD}[Note].

Note Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

(b) AV_{SS}

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

(c) V_{DD}

V_{DD} is the positive power supply pin other than P20 to P27.

(d) V_{SS}

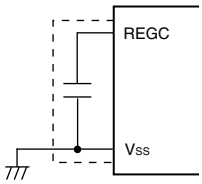
V_{SS} is the ground potential pin other than P20 to P27.

2.5.12 $\overline{RESET}$

This is the active-low system reset input pin.

2.5.13 REGC

This is the pin for connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect this pin
<R> to Vss via a capacitor (0.47 to 1 μF).



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2.5.14 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to Vss in the normal operation mode.

In flash memory programming mode, connect this pin to the flash programmer.

2.5.15 HDR

This is an output pin for high side driver.

Each driver output can control with the HDC input signal.

2.5.16 HDC

These are input pins for high side driver.

These pin have a pull-down resistor inside the IC.

Table 2-2. Truth Table

HDC	HDR
High	High
Low	Hi-Z

2.5.17 GND1, GND2

GND1 is a power supply circuit GND.

GND2 is an LIN transceiver circuit GND.

Connect GND1 and GND2 to the same potential as Vss and AVss.

2.5.18 HDS

This is a power supply pin for high side driver.

Connect HDS to the same potential as SUP.

2.5.19 LIN

This is a LIN Bus connection pin.

2.5.20 MSLP

This pin is used to switch the LIN transceiver between normal and sleep mode. In the normal mode the LIN transceiver goes into sleep mode when MSLP is set to low and in the sleep mode the LIN transceiver goes into normal mode when MSLP is set to high.

Moreover, this pin has a pull-down resistor inside the IC.

2.5.21 SUP

SUP is the positive power supply pin.

2.5.22 SWI

SWI is the high voltage input pin for external switch.

2.5.23 SWO

SWO is the SWI input signal output pin.

2.5.24 MOD1, MOD2

This pin is used as mode pin to port mode.

For details, see **6.1 LIN Transceiver Function**.

2.5.25 VRO

VRO is a voltage regulator output pin.

2.5.26 VRS

VRS is a voltage regulator output and output voltage monitor.

2.5.27 SRC

This pin is used to switch the LIN communication slew rate.

For details, see **6.1 LIN Transceiver Function**.

2.6 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuit and the recommended connections of unused pins.
Refer to Figure 2-1 for the configuration of the I/O circuits of each type.

Table 2-3. Pin I/O Circuit Types (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000	5-AQ	I/O	Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P01/TI010/TO00			
P10/$\overline{SCK10}$/TxD0			
P11/SI10/RxD0			
P12/SO10	5-AG		
P13/TxD6[Note 1]			
P14/RxD6[Note 1]	5-AQ		
P15/TOH0	5-AG		
P16/TOH1/INTP5	5-AQ		
P17/TI50/TO50/HDC[Note 2]	5-AQ, LIN-1-B		Input/Output: Connect independently to V_{SS} via a resistor.
P20/ANI0 to P27/ANI7[Note 3]	11-G		<Digital input setting and analog input setting> Independently connect to AV_{REF} or AV_{SS} via a resistor. <Digital output setting> Leave open.
P30/INTP1/SWO[Note 4]	5-AQ, LIN-2		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P31/INTP2/OCD1A[Notes 5, 6]	5-AQ		
P32/INTP3/OCD1B[Note 6]			
P33/TI51/TO51/INTP4			

Notes 1. This pin has alternate functions as LIN transceiver function pin. When this pin is used as the LIN transceiver function pin, leave it open.

2. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the HDC pin in the package analog block.

3. P20/ANI0 to P27/ANI7 are in the analog input mode after reset release.

4. These are the functions of the analog pins. The pins to which these functions are assigned are connected to the SWO pin in the package analog block.

5. Process the P31/INTP2/OCD1A and P121/X1/OCD0A pins of the products mounted with the on-chip debug function (μPD78F8032D and 78F8039D) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P31/INTP2/OCD1A	P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.	Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset		
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

6. Use the recommended connection method described above in I/O port mode when these pins are not used.

Table 2-3. Pin I/O Circuit Types (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P40, P41	5-AG	I/O	Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P60/SCL0	13-AI		Input: Connect to V_{SS}. Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDA0			
P62/EXSCL0			
P63	13-P		
P70/KR0 to P73/KR3	5-AQ		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P74, P75			
P120/INTP0/EXLVI			
P121/X1/OCD0A Notes 1, 2	37		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P122/X2/EXCLK/OCD0B Note 2			
P123/XT1 Note 2			
P124/XT2/EXCLKS Note 2			
P130	3-C	Output	Leave open.
P140/PCL/INTP6	5-AQ	I/O	Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
$\overline{\text{RESET}}$	2	Input	Connect directly to V_{DD} or via a resistor.
<R> FLMD0 Note 3	38-A	–	Connect to V_{SS}.
<R> AV_{REF}	–	–	<When one or more of P20 to P27 are set as a digital port> Make this pin the same potential as V_{DD}. <When all of P20 to P27 are set as analog ports> Make this pin to have a potential where 1.8 V ≤ AV_{REF} ≤ V_{DD}.
<R> AV_{SS}			Make this pin the same potential as V_{SS}.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).

Notes 1. Process the P31/INTP2/OCD1A and P121/X1/OCD0A pins of the products mounted with the on-chip debug function (μPD78F8032D and 78F8039D) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P31/INTP2/OCD1A	P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.	Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset		
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

2. Use the recommended connection method described above in I/O port mode when these pins are not used.

<R> **3.** FLMD0 is a pin that is used to write data to the flash memory. To rewrite the data of the flash memory on-board, connect this pin to V_{SS} via a resistor (10 kΩ: recommended). The same applies when executing on-chip debugging with a product with an on-chip debug function (μPD78F8032D and 78F8039D).

Table 2-3. Pin I/O Circuit Types (3/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
MOD1	LIN-1	Input	Connect directly to V_{SS} or VRS.
MOD2			
SRC			
SWO Note1	LIN-2	Output	Leave open
LIN	LIN-3	I/O	Leave open.
MSLP	LIN-1-A	Input	Leave open.
HDC Note2	LIN-1-B	Input	Leave open.
HDR	LIN-4	Output	Leave open.
SWI	LIN-1	Input	Connect directly to GND1.
VRO	LIN-5	Output	Connect directly to V_{DD}.
VRS		Input	Connect directly to VRO.
RxL	LIN-2	Output	– Note 3
TxL	LIN-6	Input	– Note 4
HDS	–	–	Connect directly to SUP.

Notes 1. SWO terminal is connected with P30/INTP1 in the package microcontroller block.

2. HDC terminal is connected with P17/TI50/TO50 in the package microcontroller block.

3. RxL terminal is connected with P14/RxD6 in the package microcontroller block.

4. TxL terminal is connected with P13/TxD6 in the package microcontroller block.

Figure 2-1. Pin I/O Circuit List (1/4)

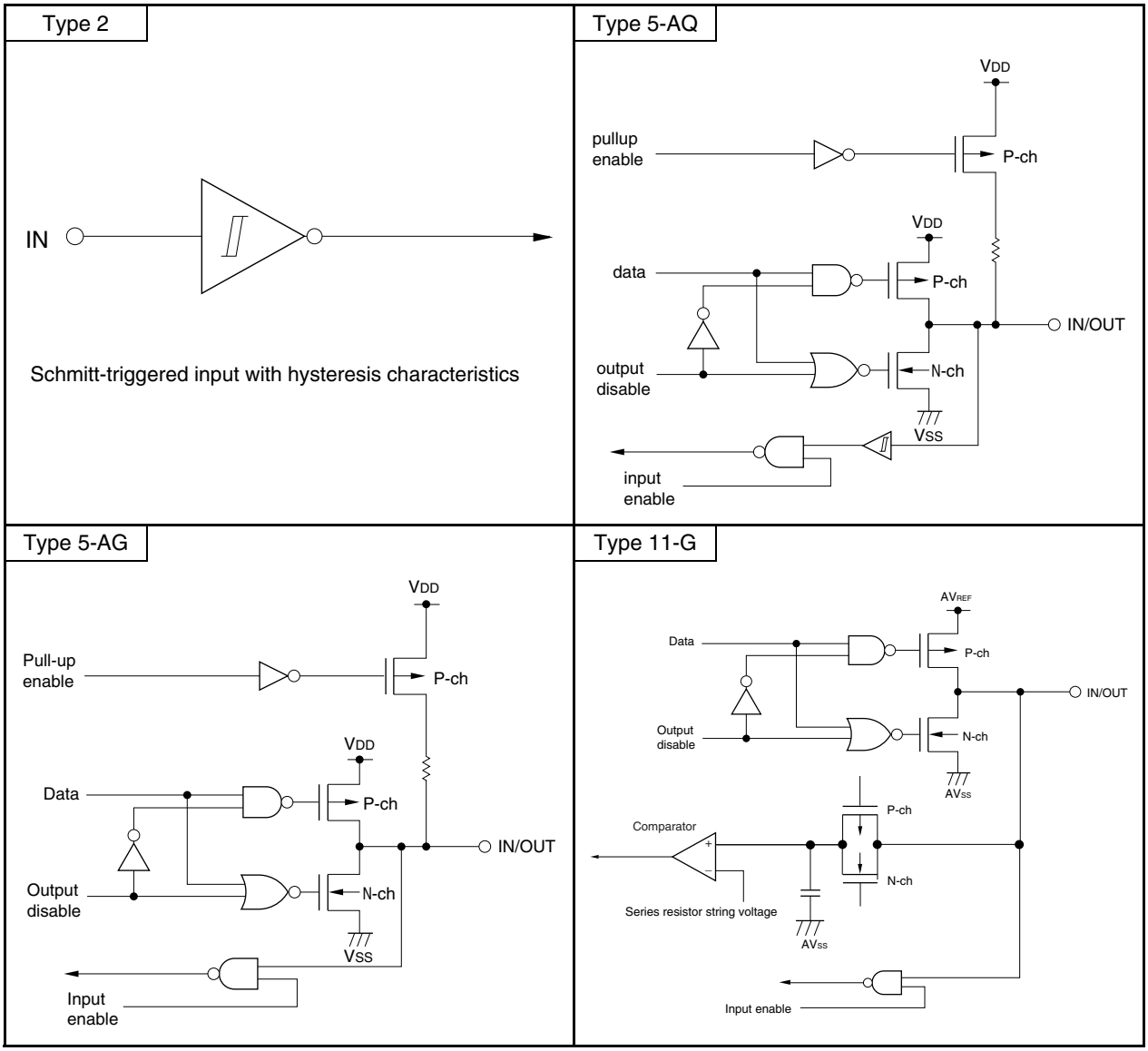
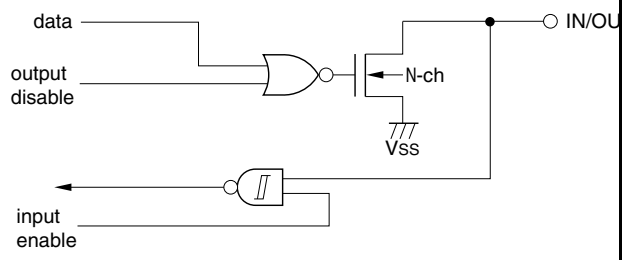
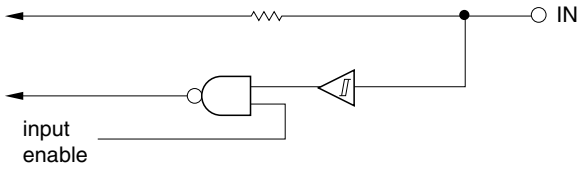


Figure 2-1. Pin I/O Circuit List (2/4)

Type 13-AI



Type 38-A



Type 37

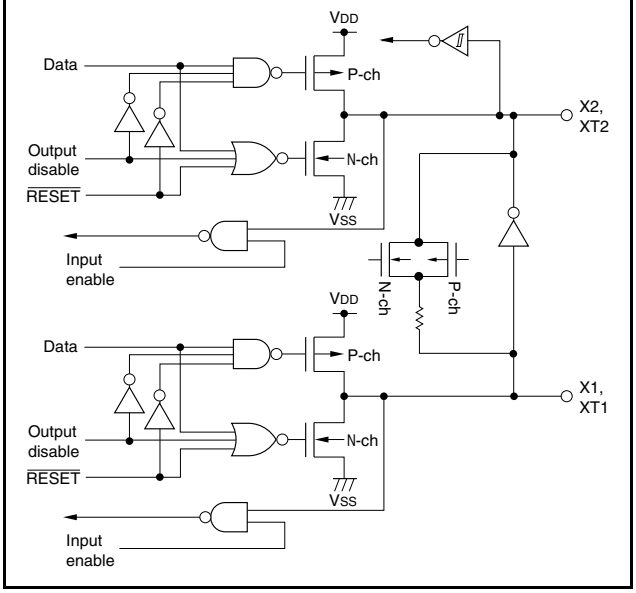
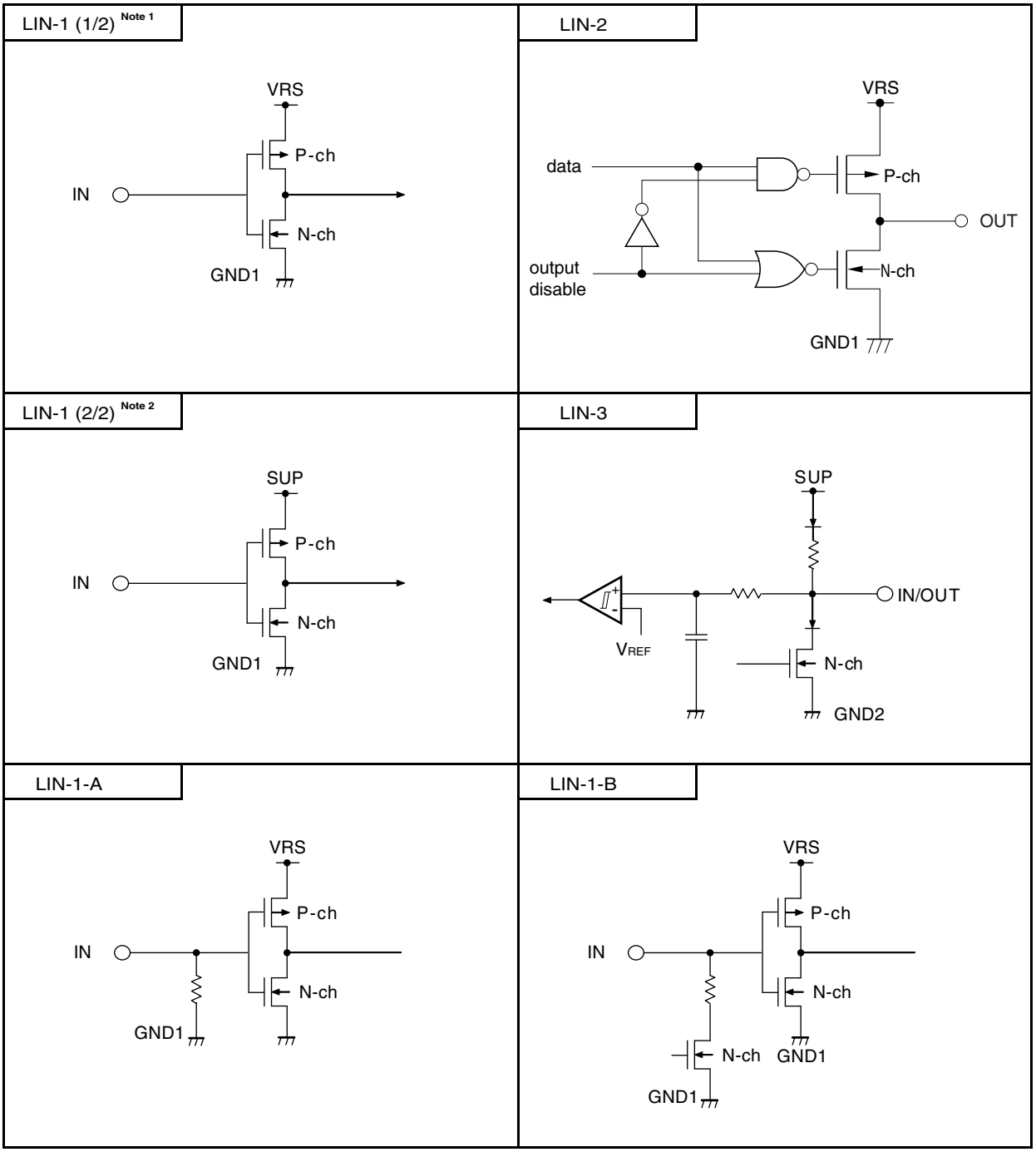


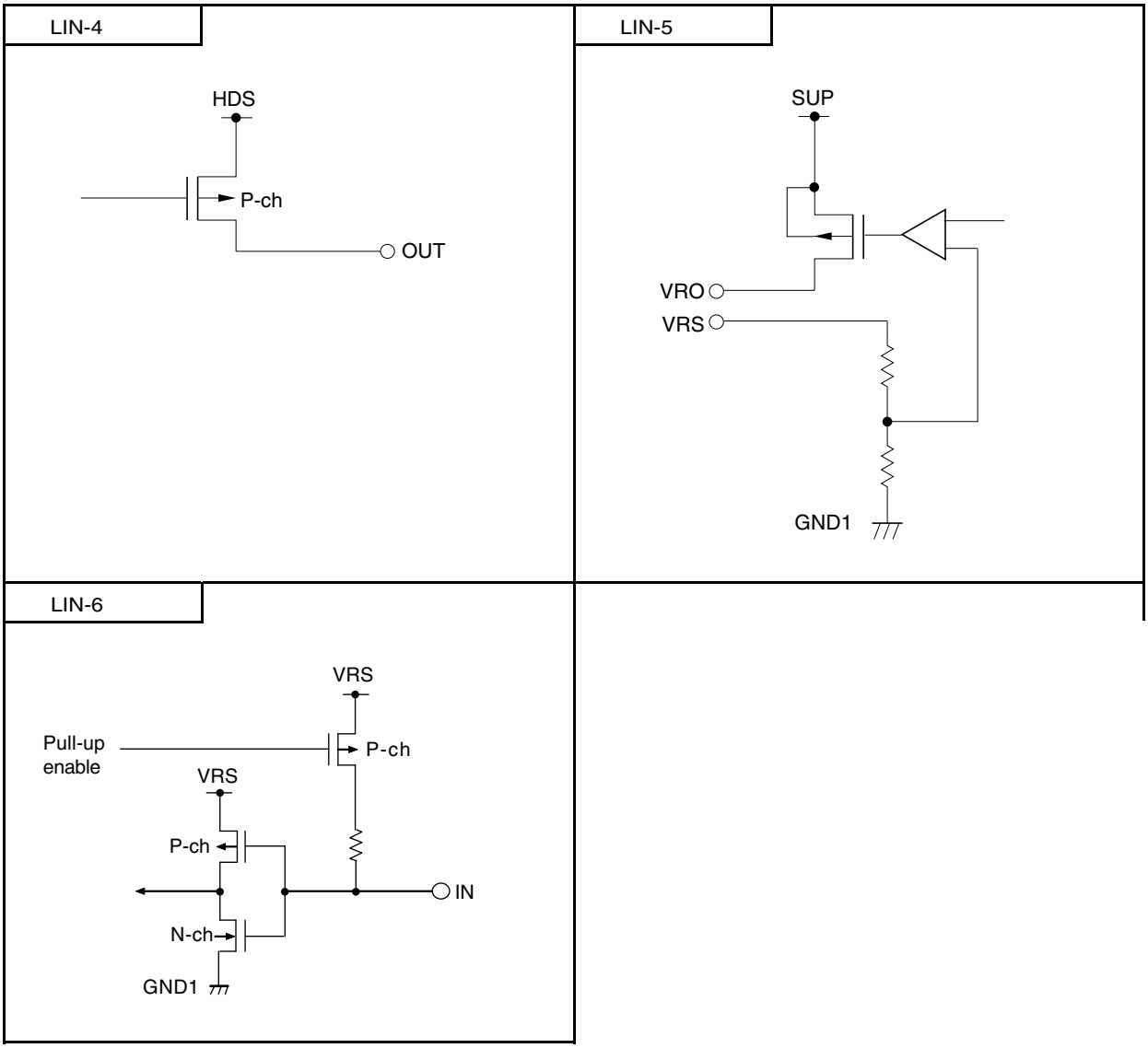
Figure 2-1. Pin I/O Circuit List (3/4)



Notes 1. MOD1, MOD2, SRC pin

2. SWI pin

Figure 2-1. Pin I/O Circuit List (4/4)



CHAPTER 3 MICROCONTROLLER FUNCTIONS

The 8-bit microcontroller is same as 78K0/KB2 or 78K0/KC2.

For detail, refer to **78K0/Kx2 User's Manual (R01UH0008E)** or **78K0/Kx2 ROM Expansion Products User's Manual (U19719E).**

CHAPTER 4 WRITING WITH FLASH PROGRAMMER

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the device has been mounted on the target system. The connectors that connect the dedicated flash programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the device is mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

Table 4-1. Wiring of Dedicated Flash Programmer

Pin Configuration of Dedicated Flash Programmer			With CSI10			With UART6		
Signal Name	I/O	Pin Function	Pin Name	Pin No.		Pin Name	Pin No.	
				48 Pin	64 Pin		48 Pin	64 Pin
SI/RxD	Input	Receive signal	SO10/P12	38	47	TxD6/P13	20	30
SO/TxD	Output	Transmit signal	SI10/RxD0/P11	39	48	RxD6/P14	19	29
SCK	Output	Transfer clock	$\overline{\text{SCK10}}$/TxD0/P10	40	49	_	_	_
CLK	Output	Clock to Micro	_ Note 1	_	_	**Note 2**	**Note 2**	**Note 2**
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	2	3	$\overline{\text{RESET}}$	2	3
FLMD0	Output	Mode signal	FLMD0	3	6	FLMD0	3	6
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	8	11	V_{DD}	8	11
			AV_{REF}	41	50	AV_{REF}	41	50
			VRO	30	38	VRO	30	38
			VRS	31	39	VRS	31	39
			HDS	26	34	HDS	26	34
			SUP	25	33	SUP	25	33
			MOD1	34	42	MOD1	34	42
V_{SS}	_	GND	V_{SS}	7	10	V_{SS}	7	10
			AV_{SS}	42	51	AV_{SS}	42	51
			GND1	13, 21 to 24, 37	31, 32, 45, 46	GND1	13, 21 to 24, 37	31, 32, 45, 46
			GND2	33	41	GND2	33	41
			MOD2	35	43	MOD2	35	43
<R>			MSLP	15	25	MSLP	15	25
			SRC	32	40	SRC	32	40
			SWI	28	36	SWI	28	36

Notes 1. Only the internal high-speed oscillation clock (f_{RH}) can be used when CSI10 is used.

2. Only the X1 clock (f_X) or external main system clock (f_{EXCLK}) can be used when UART6 is used. When using the clock out of the flash programmer, connect CLK and EXCLK of the programmer.

- PG-FP5, FL-PR5: Please connect the programmer's CLK to EXCLK/X2/P122

CHAPTER 5 POWER SUPPLY CIRCUIT

5.1 Power Supply Function

The power supply circuit is a stabilization power supply circuit that generates 5 V (TYP.) output voltage from 12 V battery supply voltage.

The power supply circuit has the following function.

- Over current protection function
- Thermal shutdown function

5.2 Power Supply Over Current Protection Function

If an overcurrent flows to the regulator output due to a cause such as a load short-circuit, this circuit controls the current and protects the device.

When the overcurrent no longer flows, the circuit recovers automatically.

Current limit = 51 mA (MIN.)

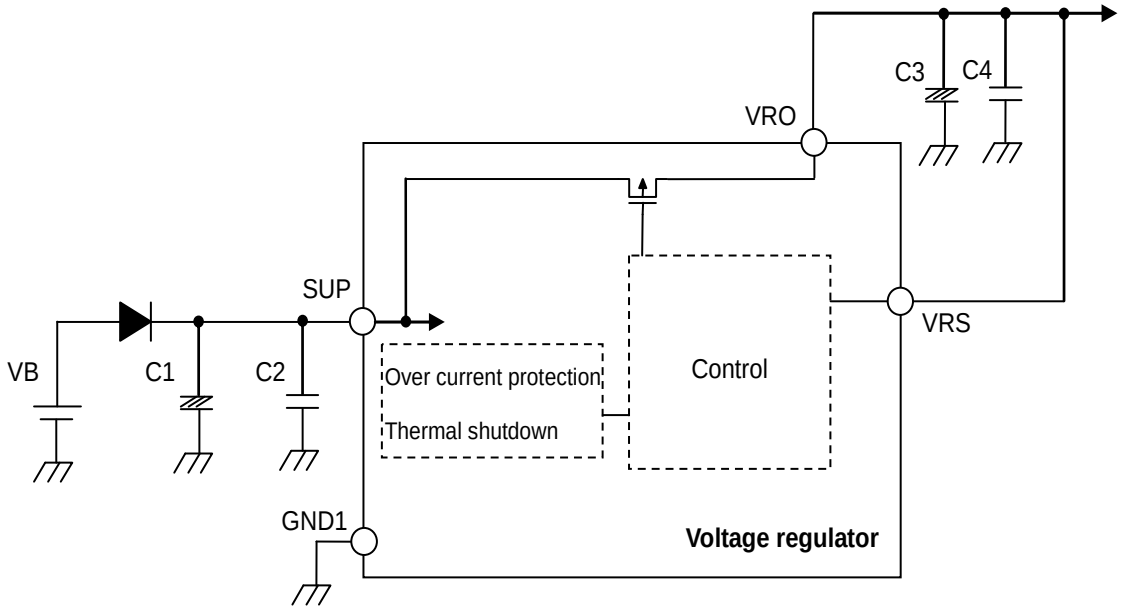
5.3 Power Supply Thermal Shutdown Function

This is a protection circuit for preventing destruction because of over temperature.

The temperature of the internal circuit is monitored and when the temperature exceeds the maximum limit the overheating detection temperature is detected and the internal P-ch MOS is forcibly switched off. After the dropper is forcibly switched off, it automatically switches back on after the temperature declines.

<R> **Caution The purpose of the built-in protection functions is to protect the device from abnormal operation. Try to avoid the use of these functions by designing the system properly. This function might degrade if the junction temperature (T_{jmax}) is exceeded continuously for a certain period of time.**

Figure 5-1. Voltage Regulator Circuit Application Example



External parts recommended

C1 ≥ 33 μF

C2 ≥ 0.01 μF

4.7 μF ≤ C3 ≤ 100 μF

C4 ≥ 0.01 μF

Caution Place the ceramic capacitor (C2, C4) between the SUP and GND pin, the VRO and GND pins adjacent to the SUP, VRO pin and use the shortest possible wiring.

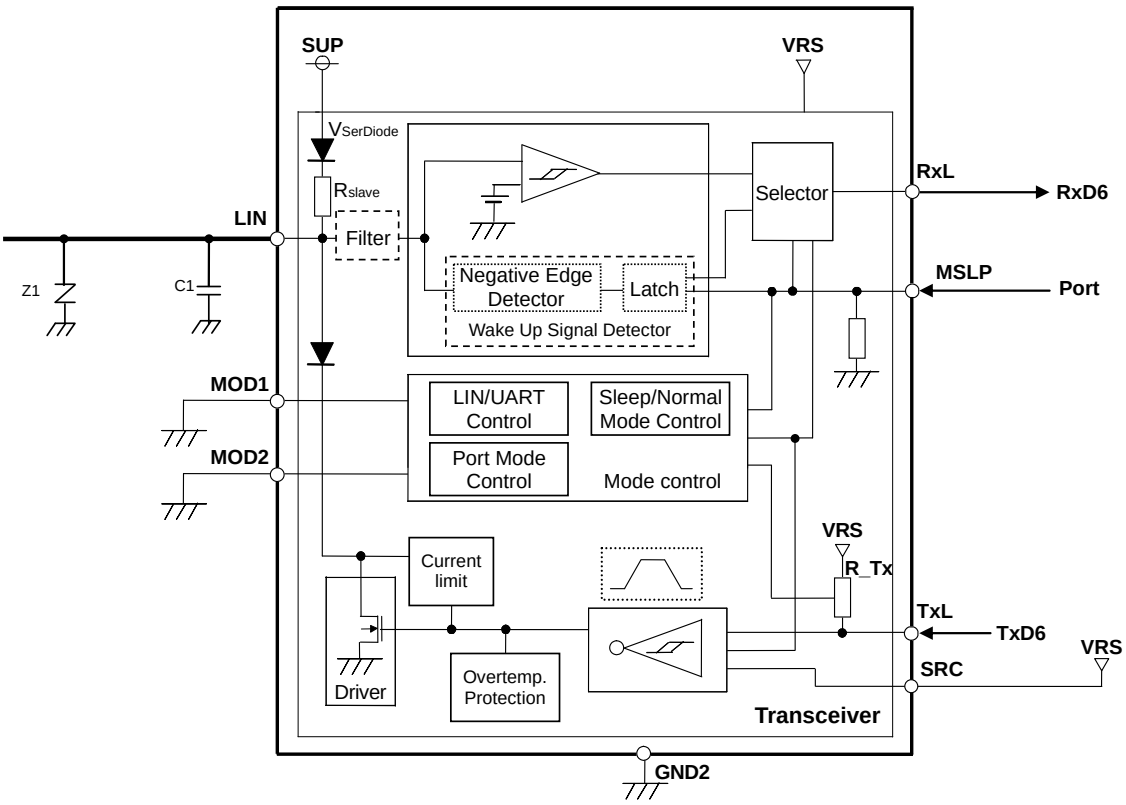
CHAPTER 6 LIN TRANSCEIVER FUNCTION

6.1 LIN Transceiver Function

<R> The LIN transceiver and external specifications comply with LIN Specifications Rev.2.0, 2.1.
The LIN transceiver has the following functions.

- Sleep function
- Over current protection function
- Thermal shutdown function

Figure 6-1. LIN Transceiver Block Diagram



Remarks 1. RxL terminal is connected to RxD6 and TxL terminal is connected to TxD6 in package.

2. LIN terminal includes slave pull-up register and diode.

6.2 Operation Mode

Figure 6-2. Operation Mode Status Transition Diagram

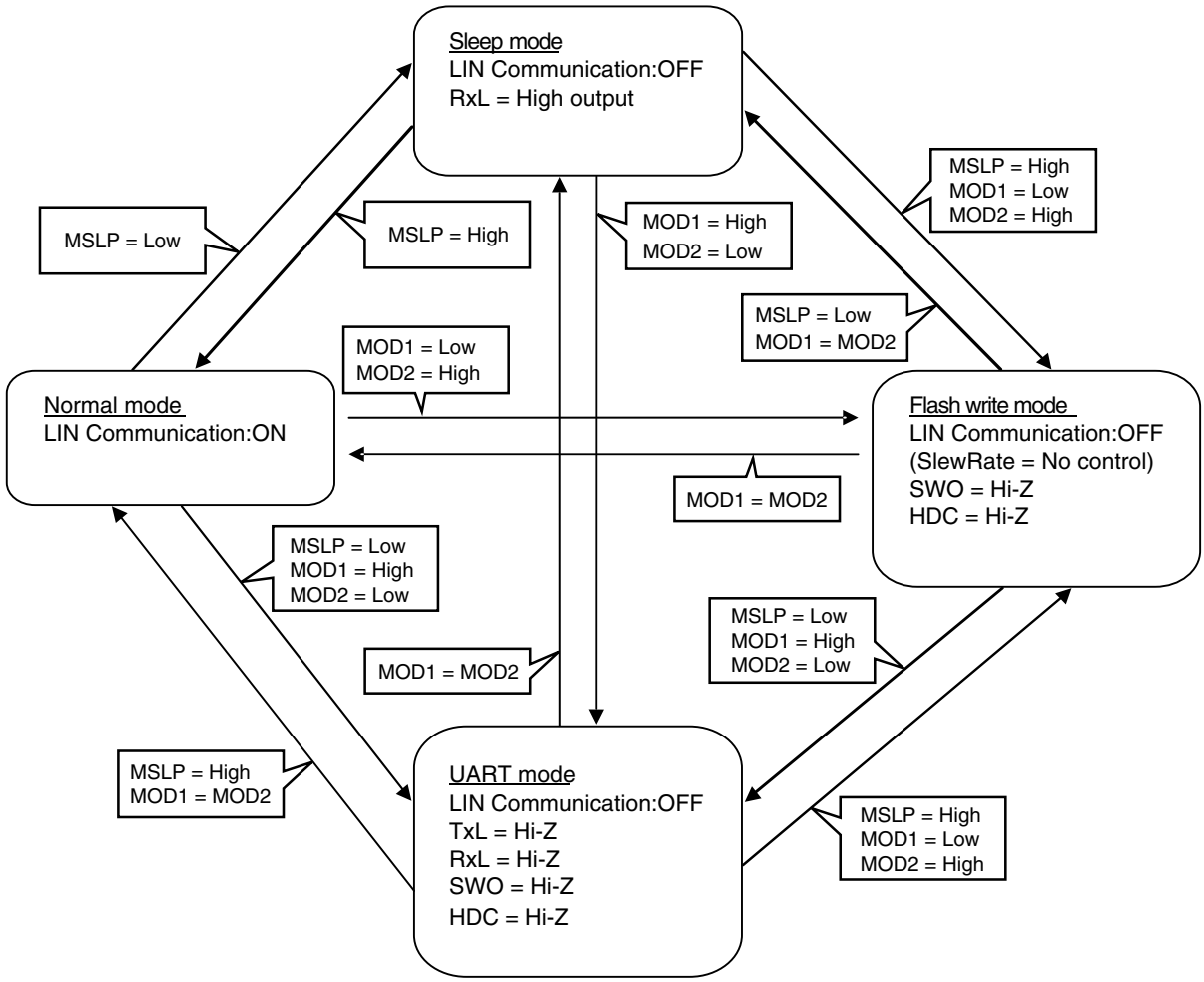


Table 6-1. LIN Operation Mode Settings

LIN Operation Mode	Slew Rate	Port Mode Note	MSLP	SRC	MOD1	MOD2
LIN sleep	–	Port mode A	L	×	L	L
		Port mode B	L	×	H	H
LIN normal	Fast	Port mode A	H	H	L	L
		Port mode B	H	H	H	H
	Slow	Port mode A	H	L	L	L
		Port mode B	H	L	H	H
Flash write	OFF	Port mode B	H	×	L	H
UART mode	–	Port mode C	L	×	H	L

Note For details about the pin statuses in the port modes, see Table 6-2 Function Pin Statuses in Each Port Mode.

Remark ×: Don't care

Table 6-2. Function Pin Statuses in Each Port Mode

Port Mode	HDC	SWO	TxL	RxL	Analog Function Status
Port mode A	Pull-down input	Output	Pull-up input	Output	The high-voltage-tolerant switch input circuit and high-side driver are usable.
Port mode B	Hi-Z	Hi-Z	Pull-up input	Output	The high-voltage-tolerant switch input circuit and high-side driver stop. (Only the pin functions of the microcontroller function block can be used for P17 and P30.)
Port mode C	Hi-Z	Hi-Z	Hi-Z	Hi-Z	The high-voltage-tolerant switch input circuit, high-side driver, and LIN transceiver stop. (Only the pin functions of the microcontroller function block can be used for P13, P14, P17, and P30.)

- Sleep mode

  If MSLP = low level and MOD1 = MOD2, the system enters the sleep mode. (The MSLP pin is internally pulled down.)

  The LIN driver output is disabled (recessive) in the sleep mode regardless of the TxL pin input status and the system enters a low-power consumption status. However, because the LIN bus is monitored in this mode, the RxL pin transitions from high level to low level when a change in the edge (from recessive to dominant) is detected for the LIN bus, a high-level signal is input to the MSLP pin, and the RxL pin retains low level until the system enters the normal mode.

- Normal mode

  If MSLP = high level and MOD1 = MOD2, the system enters the normal mode.

  If the TxL pin is set to high level in the normal mode, the LIN driver output becomes recessive. If the TxL pin is set to low level, the LIN driver becomes dominant.

  If the LIN bus becomes dominant, the RxL pin outputs a low-level signal. If the LIN bus becomes recessive, the RxL pin outputs a high-level signal.

  In the normal mode, the LIN bus can be used for communication.

  The slew rate can be changed according to the SRC pin status.

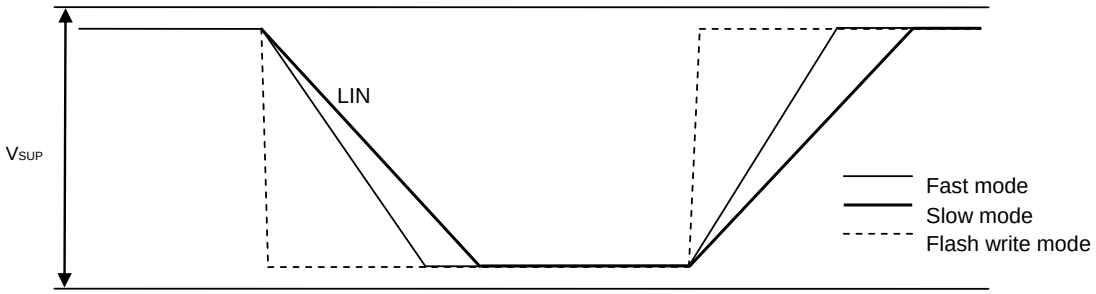
  - SRC = High … Fast mode

    Mode in which a 20 kbps communication baud rate is supported

  - SRC = Low … Slow mode

    Mode in which a 10.4 kbps communication baud rate is supported

Figure 6-2. Response Timing of Slew Rate



- Flash write mode

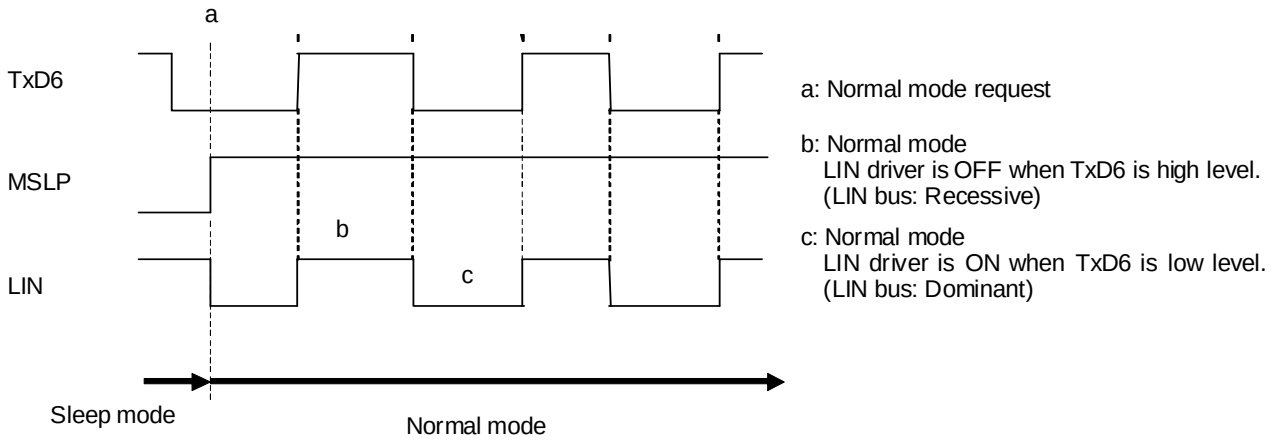
If MSLP = high level, MOD1 = low level, and MOD2 = high level, the system enters the flash write mode.
This mode supports a communication baud rate of 100 kbps and enables writing to flash ROM via the LIN bus by using high-speed communication.

Caution The flash write mode cannot be used to specify the slew rate mode.

- UART mode
  If MSLP = low level, MOD1 = high level, and MOD2 = low level, the system enters the UART mode.
  In this mode, the on-board flash ROM can be written via UART6.

Figure 6-3. Normal Mode Timing

(a) Normal mode transmitter operation (TxD6 to LIN)



(b) Normal mode receiver operation (LIN to RxD6)

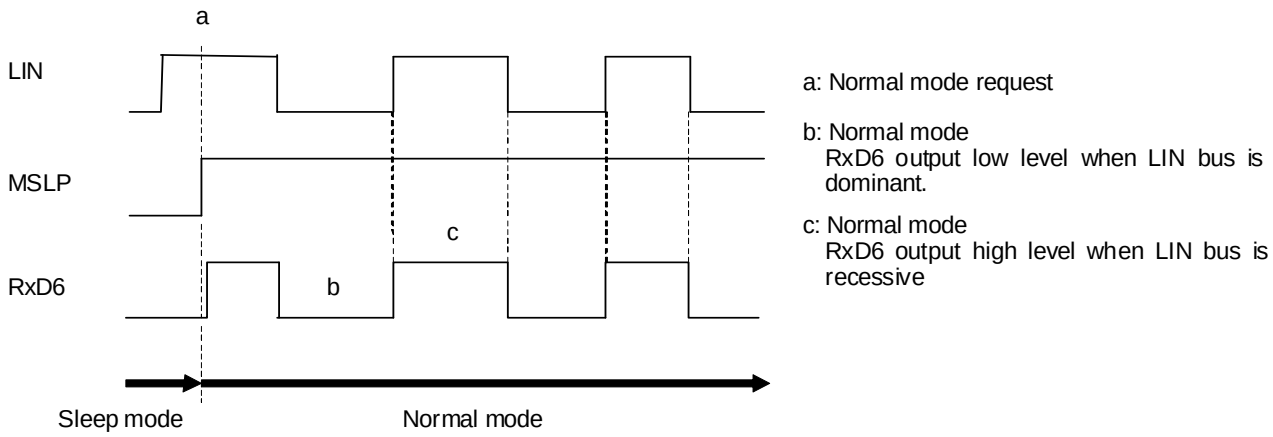
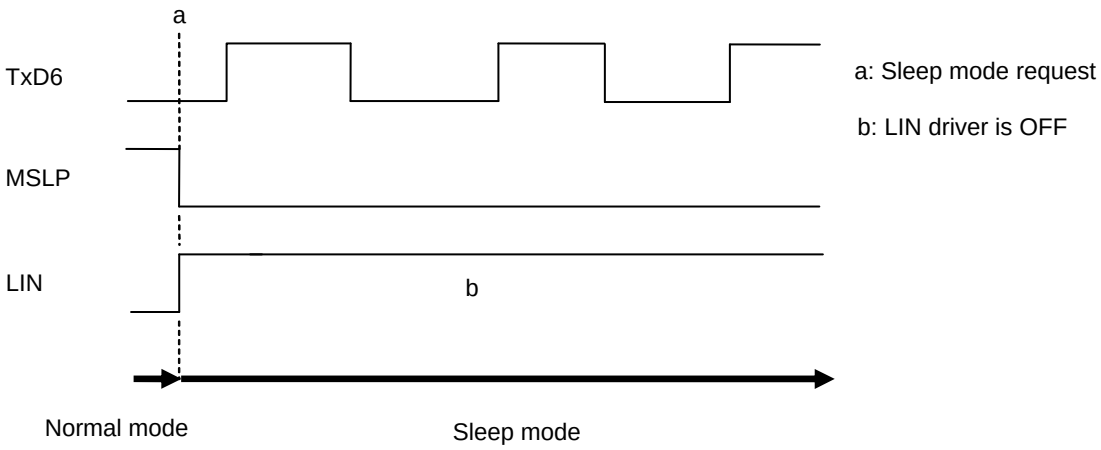
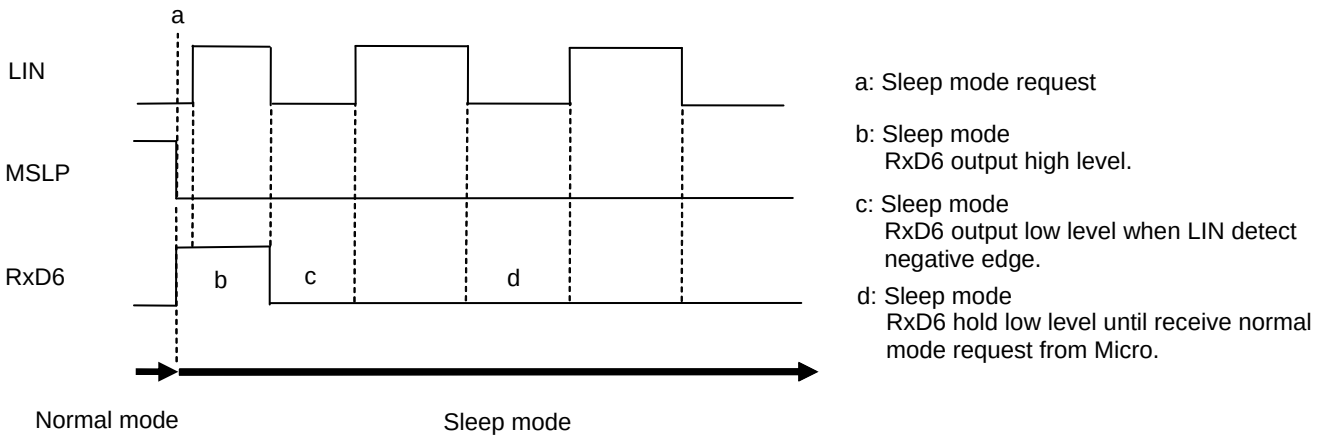


Figure 6-4. Sleep Mode Timing

(a) Sleep mode transmitter operation (TxD6 to LIN)



(b) Sleep mode transmitter operation (LIN to RxD6)



6.3 Over Current Limiter

If an overcurrent flows to the LIN driver due to a cause such as a load short-circuit, this circuit forcibly disables the LIN driver (makes it recessive) to protect it.

After an overcurrent is detected, the LIN bus is kept disabled (recessive), but can be enabled by inputting a high-level signal to the TxL pin.

Current limit = 40 mA (MIN.)

6.4 Thermal Shutdown Circuit

This is a protection circuit for preventing destruction of the device due to over temperature.

The temperature of the LIN driver is monitored and when a temperature that exceeds the overheating detection temperature (MIN: 150°C) is detected, the LIN driver is forcibly switched off. After the LIN driver is forcibly switched off, it automatically switches back on after the temperature declines.

<R> **Caution The purpose of the built-in protection functions is to protect the device from abnormal operation. Try to avoid the use of these functions by designing the system properly. This function might degrade if the junction temperature (T_{jmax}) is exceeded continuously for a certain period of time.**

CHAPTER 7 DRIVER CIRCUIT

The driver circuit has 1 channel of a high side driver circuit.
To use the high-side driver, set MOD1 and MOD2 to low level.

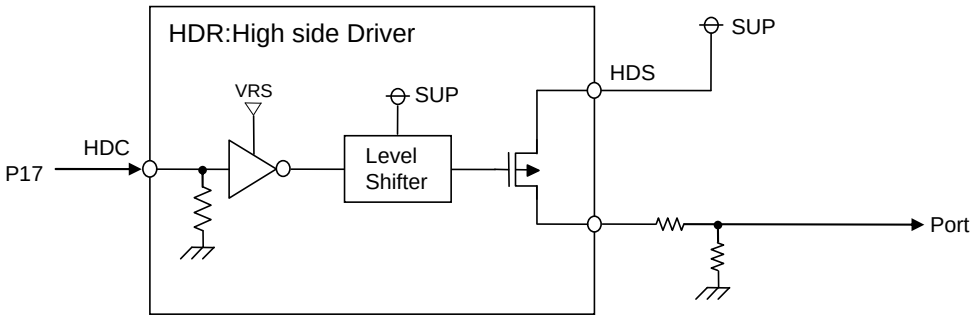
7.1 High Side Driver

- **HDR: 1 ch**
  Application: Can be used as a high-side driver for monitoring the supply voltage
  Input circuit has a pull-down resistor within the IC.

Table 7-1. Truth Table

HDC	HDR
High	High
Low	Hi-Z

Figure 7-1. High Side Driver Circuit Application Example



Caution Make SUP the same potential as HDS.

CHAPTER 8 HIGH VOLTAGE SWITCH INPUT CIRCUIT

8.1 Switch Input Function

Switch input circuit can connect 12 V battery directly.

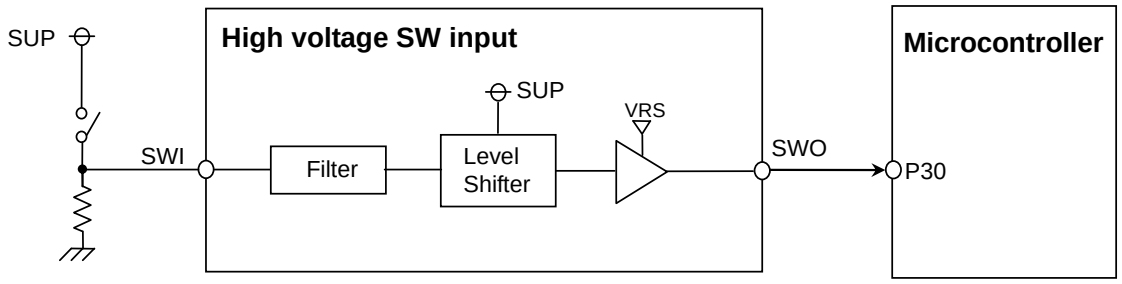
The signal input to SW1 is converted into 0 V/5 V and output.

To use the high voltage switch input function, set MOD1 and MOD2 to low level.

Table 8-1. Truth Table

SWI	SWO
High	High
Low	Low

Figure 8-1. Application Example



Remark Cut off frequency of filter = 150 kHz

CHAPTER 9 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)

Target Products	Item
48 pins	μPD78F8026(A), 78F8027(A), 78F8028(A), 78F8029(A) , 78F8030(A), 78F8032D
64 pins	μPD78F8033(A), 78F8034(A), 78F8035(A), 78F8036(A) , 78F8037(A), 78F8039D

<R> **Cautions 1. The μPD78F8032D, 78F8039D has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

2. The pins mounted depend on the product as follows.

(1) Port functions

Port	μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
	48 Pins	64 Pins
Port 0	P00, P01	
Port 1	P10 to P17	
Port 2	P20 to P23	P20 to P27
Port 3	P30 to P33	
Port 4	–	P40, P41
Port 6	P60, P61	P60 to P63
Port 7	–	P70 to P75
Port 12	P120 to P122	P120 to P124
Port 13	–	P130
Port 14	–	P140

(The remaining table is on the next page.)

(2) Non-port functions

<R>

Function		μPD78F8026 to 78F8030, 78F8032D	μPD78F8033 to 78F8037, 78F8039D
		48 Pins	64 Pins
Power supply, ground		V_{DD}, AV_{REF}, V_{SS}, AV_{SS}	
Regulator		REGC	
Reset		$\overline{RESET}$	
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS
Writing to flash memory		FLMD0	
Interrupt		INTP0 to INTP5	INTP0 to INTP6
Key interrupt		–	KR0 to KR3
Timer	TM00	TI000, TI010, TO00	
	TM50	TI50, TO50	
	TM51	TI51, TO51	
	TMH0	TOH0	
	TMH1	TOH1	
Serial interface	UART0	RxD0, TxD0	
	UART6	RxD6, TxD6	
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0
	CSI10	$\overline{SCK10}$, SI10, SO10	
A/D converter		ANI0 to ANI3	ANI0 to ANI7
Clock output		–	PCL
Low-voltage detector (LVI)		EXLVI	
On-chip debug function		OCD0A, OCD1A, OCD0B, OCD1B (mounted only onto μPD78F8032D and 78F8039D (products with on-chip debug function))	
Power Supply		SUP, VRO, VRS	
LIN transceiver		LIN, SRC, MOD1, MOD2	
Driver		HDC, HDR, HDS	
High voltage switch input		SWI, SWO	

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

9.1 Absolute Maximum Ratings

Absolute Maximum Ratings for Microcontroller Block (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD}+0.3 Note	V
	AV_{SS}		−0.5 to +0.3	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P20 to P27, P30 to P33, P40, P41, P70 to P75, P120 to P124, P140, X1, X2, XT1, XT2, RESET, FLMD0	−0.3 to V_{DD}+0.3	V
	V_{I2}	P60 to P63 (N-ch open drain)	−0.3 to +6.5	V
REGC pin input voltage	V_{IREGC}		−0.5 to +3.6 and −0.5 to V_{DD}	V
Output voltage	V_O		−0.3 to V_{DD}+0.3 Note	V
Analog input voltage	V_{AN}	ANI0 to ANI7	−0.3 to AV_{REF}+0.3 Note and −0.3 to V_{DD}+0.3 Note	V

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings for Microcontroller Block (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00, P01, P10 to P17, P30 to P33, P40, P41, P70 to P75, P120, P130, P140	−10	mA
		Total of all pins −80 mA	P00, P01, P40, P41, P120, P130, P140	−25	mA
			P10 to P17, P30 to P33, P70 to P75	−55	
	I_{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	
	I_{OH3}	Per pin	P121 to P124	−1	mA
		Total of all pins		−4	
Output current, low	I_{OL1}	Per pin	P00, P01, P10 to P17, P30 to P33, P40, P41, P60 to P63, P70 to P75, P120, P130, P140	30	mA
		Total of all pins 200 mA	P00, P01, P40, P41, P120, P130, P140	60	mA
			P10 to P17, P30 to P33, P60 to P63, P70 to P75	140	
	I_{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	
	I_{OL3}	Per pin	P121 to P124	4	mA
		Total of all pins		10	

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

Absolute Maximum Ratings for Analog Block (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{SUP1}	SUP, HDS, 400 ms	−0.3 to +60	V
	V_{SUP2}	SUP, HDS	−0.3 to +40	V
Input voltage	V_{IA1}	LIN, SWI, 400 ms	−0.3 to +60	V
	V_{IA2}	LIN, SWI	−0.3 to +40	V
	V_{IA3}	VRS	−0.3 to +6	V
	V_{IA4}	MOD1, MOD2, MSLP, HDC, SRC, TxL	−0.3 to VRS+0.3	V
LIN negative voltage	V_{ILlin}	LIN, 7 V≦VSUP≦19 V, 1 s	VSUP−40	V
Output voltage	V_{OA1}	LIN, HDR, 400 ms	−0.3 to +60	V
	V_{OA2}	LIN, HDR	−0.3 to +40	V
	V_{OA3}	VRO	−0.3 to +6	V
	V_{OA4}	SWO, RxL	−0.3 to VRS+0.3	V
Output current	I_{RO}	VRO	Self limit Note	mA
	I_{LIN}	LIN	Self limit Note	mA
<R>	I_{HDR}	HDR	25	mA
	I_{RX}	RxL	−10 to +10	mA
<R>	I_{SWO}	SWO	−10 to +10	mA

Note Current value that is limited by over current limitation circuit.

Absolute Maximum Ratings for Common Item (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Operation ambient temparatuer	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_{jmax}		150	°C

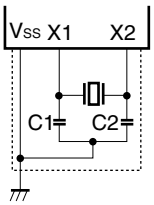
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

9.2 Microcontroller Block Characteristics

X1 Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator, crystal resonator		X1 clock oscillation frequency (f_X)Note 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0Note 2		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		5.0	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

Internal Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

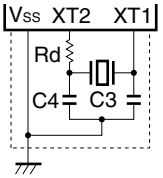
Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
8 MHz internal oscillator	Internal high-speed oscillation clock frequency (f_{RH})[Note]	RSTS = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	7.6	8.0	8.4	MHz
			1.8 V ≤ V_{DD} < 2.7 V	7.6	8.0	10.4	MHz
		RSTS = 0		2.48	5.6	9.86	MHz
240 kHz internal oscillator	Internal low-speed oscillation clock frequency (f_{RL})	2.7 V ≤ V_{DD} ≤ 5.5 V		216	240	264	kHz
		1.8 V ≤ V_{DD} < 2.7 V		192	240	264	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Remark RSTS: Bit 7 of the internal oscillation mode register (RCM))

XT1 Oscillator Characteristics[Note 1]

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})[Note 2]		32	32.768	35	kHz

Notes 1. The 48 pin products is not provided with the XT1 oscillator.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

DC Characteristics (1/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00, P01, P10 to P17, P30 to P33, P40, P41, P70 to P75, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–2.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Total[Note 2] of P00, P01, P40, P41, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V			–12.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–7.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total[Note 2] of P10 to P17, P30 to P33, P70 to P75	4.0 V ≤ V_{DD} ≤ 5.5 V			–18.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total[Note 2] of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			–23.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–20.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–15.0	mA
	I_{OH2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			–0.1	mA
		Per pin for P121 to P124				–0.1	mA
Output current, low[Note 2]	I_{OL1}	Per pin for P00, P01, P10 to P17, P30 to P33, P40, P41, P70 to P75, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Per pin for P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total[Note 3] of P00, P01, P40, P41, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total[Note 3] of P10 to P17, P30 to P33, P60, to P63, P70 to P75	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			50.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			0.4	mA
		Per pin for P121 to P124				0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<R> <Example> Where the duty factor is 50%, I_{OH} = –20.0 mA

Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

DC Characteristics (2/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high (products whose flash memory is at least 48 KB)[Note 1]	V_{IH1}	P12, P13, P15, P40, P41, P121 to P124		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P75, P120, P140, RESET, EXCLK, EXCLKS		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	P60 to P63		0.7V_{DD}		6.0	V
Input voltage, high (products whose flash memory is less than 32 KB)[Note 2]	V_{IH1}	P12, P13, P15, P40, P41, P121 to P124		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P75, P120, P140, RESET, EXCLK, EXCLKS		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	P60 to P63		0.7V_{DD}		6.0	V
Input voltage, low (products whose flash memory is at least 48 KB)[Note 1]	V_{IL1}	P12, P13, P15, P40, P41, P60 to P63, P121 to P124		0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P75, P120, P140, RESET, EXCLK, EXCLKS		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Input voltage, low (products whose flash memory is less than 32 KB)[Note 2]	V_{IL1}	P12, P13, P15, P40, P41, P60 to P63, P121 to P124		0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P75, P120, P140, RESET, EXCLK, EXCLKS		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Output voltage, high	V_{OH1}	P00, P01, P10 to P17, P30 to P33, P40, P41, P70 to P75, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = –100 μA	V_{DD} – 0.5			V
		P121 to P124	I_{OH2} = –100 μA	V_{DD} – 0.5			V

Notes 1. Supported products: 48-pin products and 64-pin products whose flash memory is at least 48 KB

2. Supported products: 48-pin products and 64-pin products whose flash memory is less than 32 KB

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

DC Characteristics (3/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P00, P01, P10 to P17, P30 to P33, P40, P41, P70 to P75, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA				0.7	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 1.0 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA				0.4	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA				0.4	V
		P121 to P124	I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA				0.6	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 3.0 mA				0.4	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA				0.4	V
Input leakage current, high	I_{LIH1}	P00, P01, P10 to P17, P30 to P33, P40, P41, P60 to P63, P70 to P75, P120, P130, P140, FLMD0, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH2}	P20 to P27	V_I = AV_{REF} = V_{DD}				1	μA
	I_{LIH3}	P121 to 124 (X1, X2, XT1, XT2)	V_I = V_{DD}	I/O port mode			1	μA
				OSC mode			20	μA
Input leakage current, low	I_{LIL1}	P00, P01, P10 to P17, P30 to P33, P40, P41, P60 to P63, P70 to P75, P120, P130, P140, FLMD0, $\overline{\text{RESET}}$	V_I = V_{SS}				–1	μA
	I_{LIL2}	P20 to P27	V_I = V_{SS}, AV_{REF} = V_{DD}				–1	μA
	I_{LIL3}	P121 to 124 (X1, X2, XT1, XT2)	V_I = V_{SS}	I/O port mode			–1	μA
				OSC mode			–20	μA
Pull-up resistor	R_U	V_I = V_{SS}			10	20	100	kΩ
FLMD0 supply voltage	V_{IL}	In normal operation mode			0		0.2 V_{DD}	V
	V_{IH}	In self-programming mode			0.8 V_{DD}		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

	Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
<R>	Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	5.5	mA
					Resonator connection		4.5	6.9	mA
				f_{XH} = 20 MHz, V_{DD} = 3.0 V [Note 2]	Square wave input		3.2	5.5	mA
					Resonator connection		4.2	6.6	mA
				f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	2.8	mA
					Resonator connection		2.3	3.9	mA
				f_{XH} = 10 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	2.7	mA
					Resonator connection		2.2	3.2	mA
				f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	1.6	mA
					Resonator connection		1.3	2.0	mA
				f_{XH} = 5 MHz, V_{DD} = 2.0 V [Notes 2, 3]	Square wave input		0.7	1.4	mA
					Resonator connection		1.0	1.6	mA
				f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	2.5	mA
				f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5, 6]	Square wave input		6	30	μA
					Resonator connection		15	35	μA
		I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	2.6	mA
					Resonator connection		2.0	4.4	mA
				f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	1.3	mA
					Resonator connection		1.0	2.4	mA
				f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	0.65	mA
					Resonator connection		0.5	1.1	mA
				f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.2	mA
				f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5, 6]	Square wave input		3.0	27	μA
					Resonator connection		12	32	μA
<R>		I_{DD3}[Note 7]	STOP mode				1	20	μA
				V_{DD} = 5.0 V, T_A = −40 to +70°C			1	10	μA
<R>	A/D converter operating current	I_{ADC}[Note 8]	2.3 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	1.9	mA
	Watchdog timer operating current	I_{WDT}[Note 9]	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
	LVI operating current	I_{LVI}[Note 10]					9	18	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

(Notes on next page)

Notes 1. Total current flowing into the internal power supply (V_{DD}), including the peripheral operation current and the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, the current flowing into the pull-up resistors and the output current of the port are not included.

2. Not including the operating current of the 8 MHz internal oscillator, 240 kHz internal oscillator, and XT1 oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

3. When AMPH (bit 0 of clock operation mode select register (OSCCTL)) = 0.

4. Not including the operating current of the X1 oscillator, XT1 oscillator, and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

5. Not including the operating current of the X1 oscillation, 8 MHz internal oscillator and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

6. Subsystem clock is μPD78F8033 to 78F8037, 78F8039D only.

7. Not including the operating current of the 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

8. Current flowing only to the A/D converter (AV_{REF}). The current value of the microcontroller block is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

9. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the microcontroller block is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

10. Current flowing only to the LVI circuit. The current value of the microcontroller block is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

AC Characteristics

(1) Basic operation (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
			1.8 V ≤ V_{DD} < 2.7 V	0.4 Note 1		32	μs
		Subsystem clock (f_{SUB}) operation Note 2		114	122	125	μs
<R> Peripheral hardware clock frequency	f_{PRS}	f_{PRS} = f_{XH}(XSEL = 1)	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
			2.7 V ≤ V_{DD} < 4.0 V Note 3			20	MHz
			1.8 V ≤ V_{DD} < 2.7 V			5	MHz
		f_{PRS} = f_{RH}(XSEL = 0)	2.7 V ≤ V_{DD} < 4.0 V	7.6		8.4	MHz
			1.8 V ≤ V_{DD} < 2.7 V Note 4	7.6		10.4	MHz
External main system clock frequency	f_{EXCLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.0 Note 5		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V		1.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}	2.7 V ≤ V_{DD} ≤ 5.5 V		24			ns
		1.8 V ≤ V_{DD} < 2.7 V		96			ns
External subsystem clock frequency Note 2	f_{EXCLKS}			32	32.768	35	kHz
External subsystem clock input high-level width, low-level width Note 2	$t_{EXCLKSH}$, $t_{EXCLKSL}$			12			μs
TI000, TI010 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V		2/f_{sam} + 0.1 Note 6			μs
		2.7 V ≤ V_{DD} < 4.0 V		2/f_{sam} + 0.2 Note 6			μs
		1.8 V ≤ V_{DD} < 2.7 V		2/f_{sam} + 0.5 Note 6			μs
TI50, TI51 input frequency	f_{TI5}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				10	MHz
		1.8 V ≤ V_{DD} < 2.7 V				5	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}	4.0 V ≤ V_{DD} ≤ 5.5 V		50			ns
		2.7 V ≤ V_{DD} < 4.0 V		50			ns
		1.8 V ≤ V_{DD} < 2.7 V		100			ns

Notes 1. 0.38 μs when operating with the 8 MHz internal oscillator.

2. Subsystem clock is μPD78F8033 to 78F8037, 78F8039D only.

3. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{XH}/2 (10 MHz) or less. The multiplier/divider, however, can operate on f_{XH} (20 MHz).

4. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{RH}/2 or less.

5. 2.0 MHz (MIN.) when using UART6 during on-board programming.

6. Selection of f_{sam} = f_{PRS}, f_{PRS}/4, f_{PRS}/256, is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode registers 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, f_{sam} = f_{PRS}.

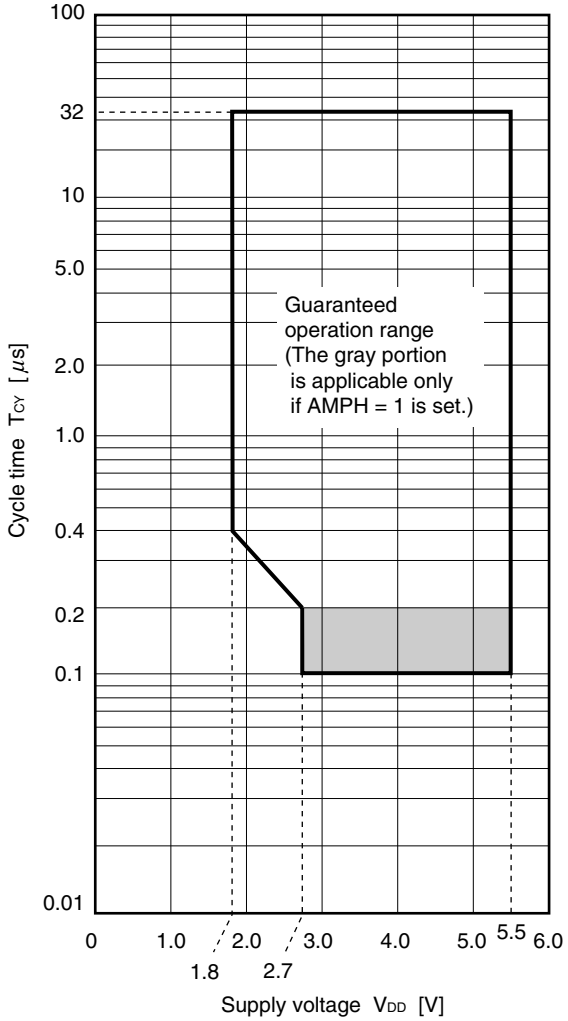
<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

(1) Basic operation (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

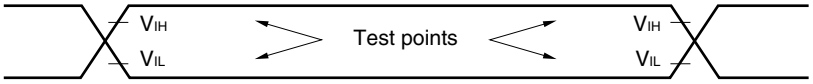
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}		1			μs
Key interrupt input low-level width	t_{KR}		250			ns
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD} (Main System Clock Operation)

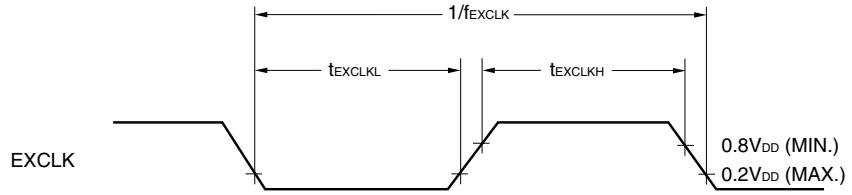


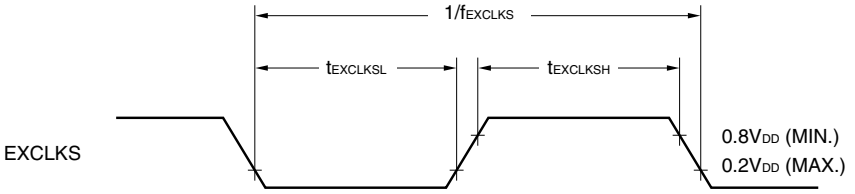
<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

AC Timing Test Points

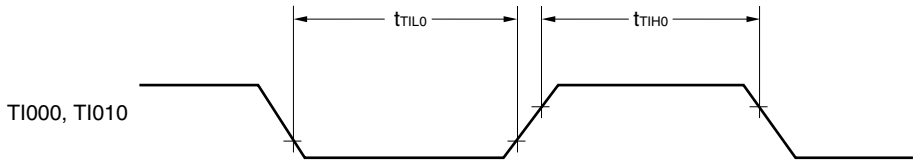


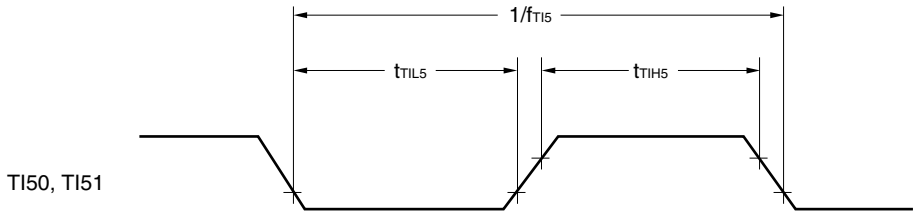
External Main System Clock Timing, External Subsystem Clock Timing



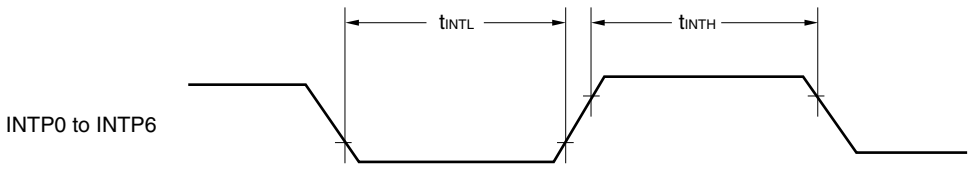


TI Timing



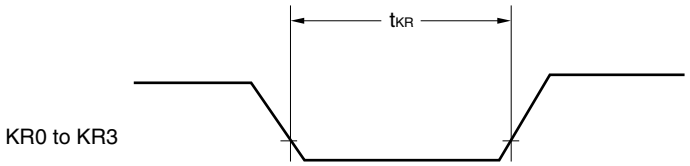


Interrupt Request Input Timing

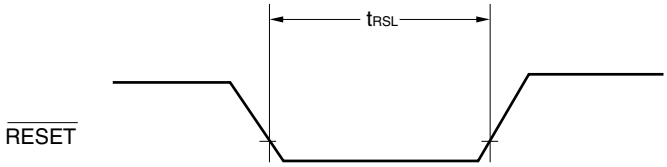


<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(2) Serial interface

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

(a) UART6 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

(c) IIC0

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{CLK}		0	100	0	400	kHz
Reset condition setup time	$t_{SU:STA}$		4.7		0.6		μs
Hold time Note 1	$t_{HD:STA}$		4.0		0.6		μs
Hold tome when SCL0 = "L"	t_{LOW}	Internal clock operation	4.7		1.3		μs
		EXSCL0 clock (6.4 MHz) operation	4.7		1.25		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	$f_W = f_{XH}/2^N$ or $f_W = f_{EXSCL0}$ selected Note 3	0	3.45	0	0.9 Note 4	μs
						1.00 Note 5	μs
		$f_W = f_{RH}/2^N$ selected Note 3	0	3.45	0	1.05	μs
Stop condition setup time	$t_{SU:STO}$		4.0		0.6		μs
Bus free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/reset condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

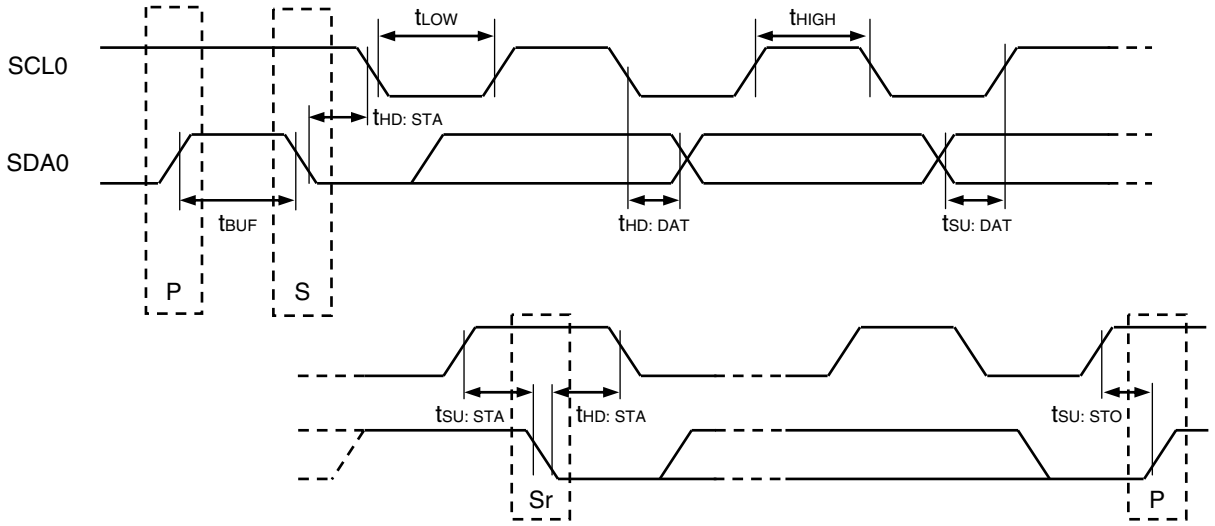
3. f_W indicates the IIC0 transfer clock selected by the IICCL0 and IICX0 registers.

4. When $f_W \geq 4.4$ MHz is selected

5. When $f_W < 4.4$ MHz is selected

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

IIC0 Transfer Timing



P : Stop condition
S : Start condition
Sr : Restart condition

(d) CSI10 (master mode, $\overline{SCK10}$... internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	200			ns
		2.7 V ≤ V_{DD} < 4.0 V	400			ns
		1.8 V ≤ V_{DD} < 2.7 V	600			ns
$\overline{SCK10}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2 - 20$ Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V	$t_{KCY1}/2 - 30$ Note 1			ns
		1.8 V ≤ V_{DD} < 2.7 V	$t_{KCY1}/2 - 60$ Note 1			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	70			ns
		2.7 V ≤ V_{DD} < 4.0 V	100			ns
		1.8 V ≤ V_{DD} < 2.7 V	190			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI1}		30			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO1}	C = 50 pF Note 2			40	ns

Notes1. This value is when high-speed system clock (f_{XH}) is used.

2. C is the load capacitance of the $\overline{SCK10}$ and SO10 output lines.

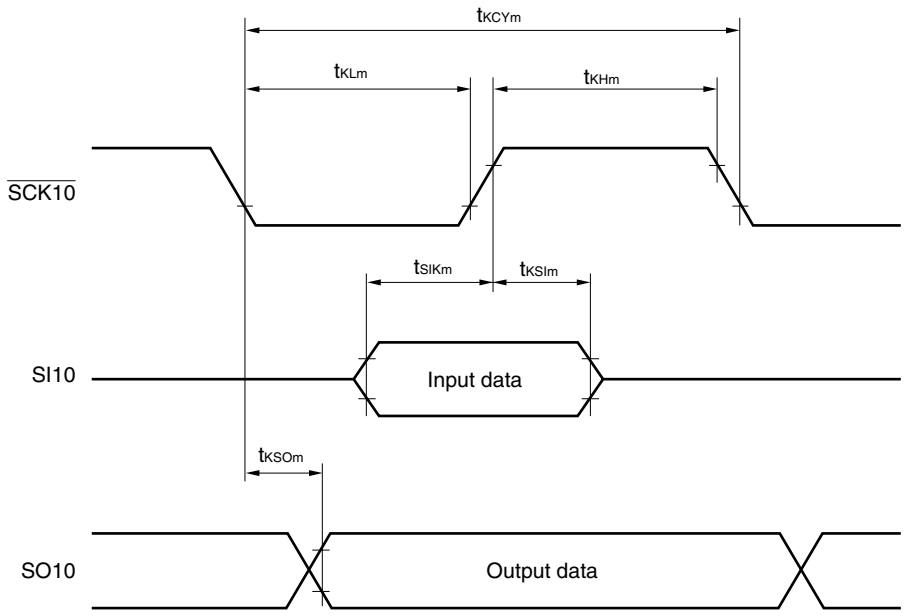
<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

(e) CSI10 (slave mode, $\overline{\text{SCK10}}$... external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK10}}$ cycle time	t_{KCY2}			400			ns
$\overline{\text{SCK10}}$ high-/low-level width	t_{KH2}, t_{KL2}			$t_{KCY2}/2$			ns
SI10 setup time (to $\overline{\text{SCK10}}$↑)	t_{SIK2}			80			ns
SI10 hold time (from $\overline{\text{SCK10}}$↑)	t_{KSI2}			50			ns
Delay time from $\overline{\text{SCK10}}$↓ to SO10 output	t_{KSO2}	C = 50 pF Note	4.0 V ≤ V_{DD} ≤ 5.5 V			120	ns
			2.7 V ≤ V_{DD} < 4.0 V			120	ns
			1.8 V ≤ V_{DD} < 2.7 V			180	ns

Note C is the load capacitance of the SO10 output line.

CSI10 Transfer Timing



Remark m = 1, 2

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

A/D Converter Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				10	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		66.6	μs
		2.7 V ≤ AV_{REF} < 4.0 V	12.2		66.6	μs
		2.3 V ≤ AV_{REF} < 2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Integral non-linearity error[Note 1]	I_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±6.5	LSB
Differential non-linearity error[Note 1]	D_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±2.0	%FSR
Analog input voltage	V_{AIN}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

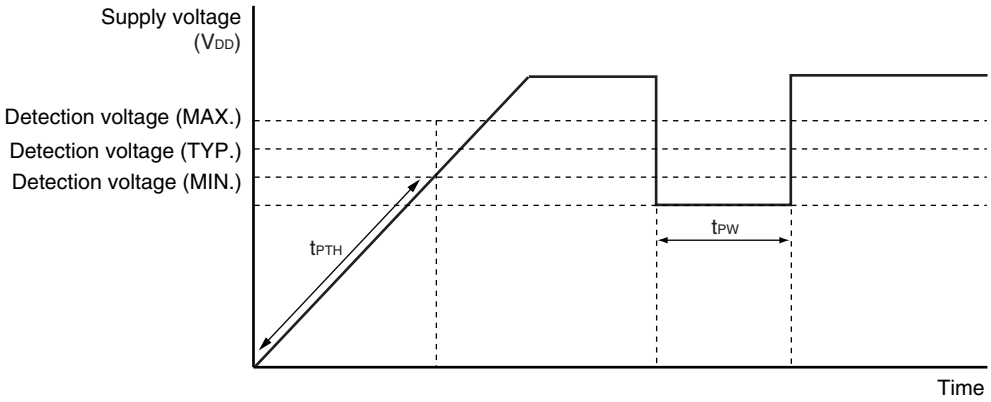
2. This value is indicated as a ratio (%FSR) to the full-scale value.

1.59 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		1.44	1.59	1.74	V
Power voltage rise inclination	t_{PTH}	V_{DD}: 0 V → change inclination of V_{POC}	0.5			V/ms
Minimum pulse width	t_{PW}		200			μs

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

POC Circuit Timing

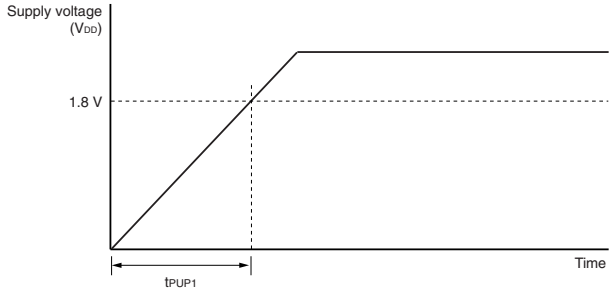


Supply Voltage Rise Time (T_A = –40 to +85°C, V_{SS} = 0 V)

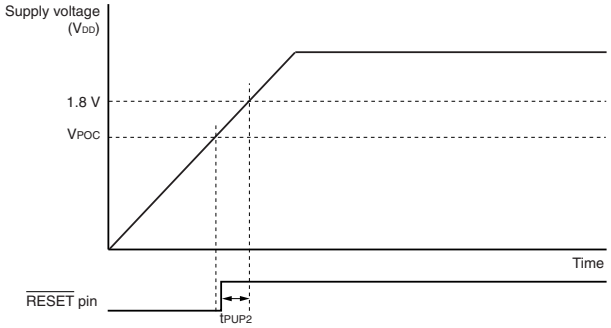
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (releasing $\overline{\text{RESET}}$ input → V_{DD}: 1.8 V)	t_{PUP2}	POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is used			1.9	ms

Supply Voltage Rise Time Timing

• When $\overline{\text{RESET}}$ pin input is not used



• When $\overline{\text{RESET}}$ pin input is used



<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

2.7 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option bye) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.

<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

LVI Circuit Characteristics (T_A = –40 to +85°C, $V_{POC} \le V_{DD} \le 5.5$ V, $AV_{REF} \le V_{DD}$, V_{SS} = 0 V)

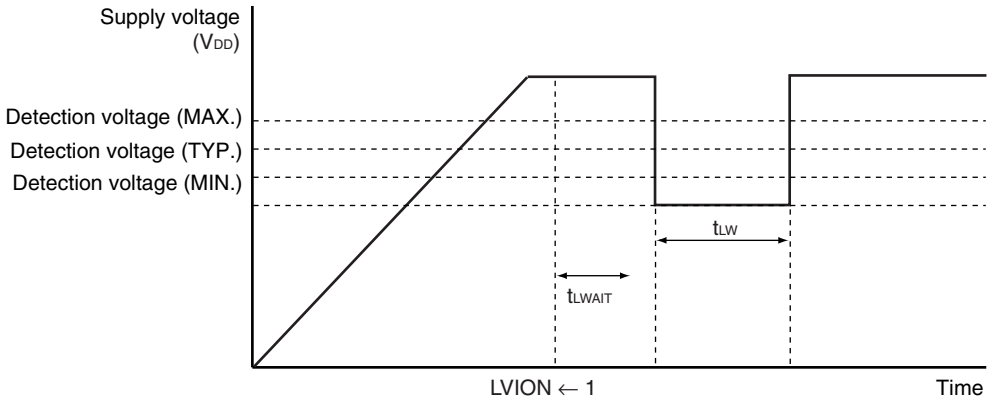
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
		V_{LVI10}		2.60	2.70	2.80	V
		V_{LVI11}		2.45	2.55	2.65	V
		V_{LVI12}		2.29	2.39	2.49	V
		V_{LVI13}		2.14	2.24	2.34	V
		V_{LVI14}		1.98	2.08	2.18	V
		V_{LVI15}		1.83	1.93	2.03	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}		10			μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

LVI Circuit Timing

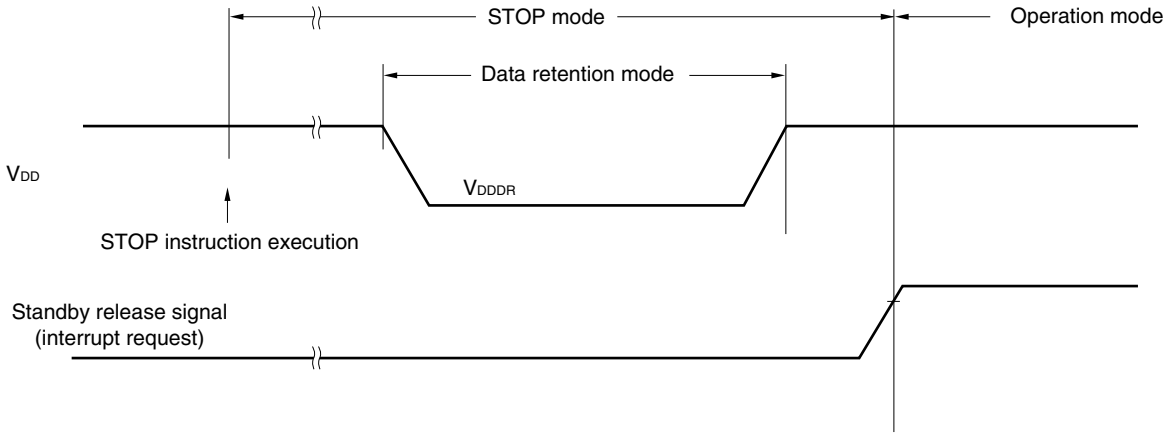


<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



<R> **Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

- **Basic characteristics**

Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)				4.5	11.0	mA
Erase time[Notes 1, 2]	All block	T_{eraca}					20	200	ms
	Block unit	T_{erasa}					20	200	ms
Write time (in 8-bit units)[Note 1]		T_{wrwa}					10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite[Note 3]	• When a flash memory programmer is used, and the libraries[Note 4] provided by Renesas Electronics are used • For program update	15 years	1000			Times
				• When the EEPROM emulation libraries[Note 5] provided by Renesas Electronics are used • The rewritable ROM size: 4 KB • For data update	5 years	10000			Times
				Conditions other than the above[Note 6]	10 years	100			Times

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP5, is used and the rewrite time during self programming, see **CHAPTER 27 FLASH MEMORY in 78K0/Kx2 User's Manual (R01UH0008E)**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

4. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual** (**U17516E**) is excluded.

5. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (**U17517E**) is excluded.

6. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual** (**U17516E**) and the sample program specified by **the 78K0/Kx2 EEPROM Emulation Application Note** (**U17517E**) are used.

Remarks 1. f_{XP}: Main system clock oscillation frequency

2. For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (U17739E)**.

9.3 Analog Block Characteristics

Voltage regulator circuit characteristics (T_A = –40 to +85°C, 6 V ≤ V_{SUP} ≤ 19 V)

<R>

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
REG output voltage	V_{CCOUT1}	7 V ≤ V_{SUP} ≤ 19 V V_{CCOUT} = VRO = VRS, I_{RO} = 1 to 50 mA	4.9	5	5.1	V
	V_{CCOUT2}	6 V ≤ V_{SUP} ≤ 19 V V_{CCOUT} = VRO = VRS, I_{RO} = 1 to 25 mA	4.75	5	5.25	V
	V_{CCOUT3}	19 V < V_{SUP} ≤ 40 V V_{CCOUT} = VRO = VRS, I_{RO} = 1 mA	4.5	5	5.5	V
Over current detect current	I_{ROlim1}	7 V ≤ V_{SUP} ≤ 19 V	51		300	mA
	I_{ROlim2}	6 V ≤ V_{SUP} < 7 V	26		300	mA
Load regulation	REG_{L1}	1 mA < I_{RO} ≤ 50 mA, V_{SUP} = 14 V			60	mV
Input regulation	REG_{IN1}	7 V ≤ V_{SUP} ≤ 19 V, I_{RO} = 50 mA			60	mV
		6 V ≤ V_{SUP} ≤ 19 V, I_{RO} = 25 mA			60	mV
Thermal shutdown	V_{Rth}		(150)			°C

Remark The values in parentheses are based on design for which no outgoing inspection has been performed.

Supply current Characteristics (T_A = –40 to +85°C, 6 V ≤ V_{SUP} ≤ 19 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{SUP1} Notes 1, 2	I_{SUP1} = I_{SUP}, LIN: Sleep, T_A = 25°C, V_{SUP} = 14 V			35	μA
	I_{SUP2} Notes 1, 2	I_{SUP2} = I_{SUP}, LIN: Sleep			60	μA
	I_{SUP3} Notes 1, 2	I_{SUP3} = I_{SUP}, LIN: Nomal (LIN bus: Recessive)			1	mA
	I_{SUP4} Note 1	I_{SUP1} = I_{SUP}, LIN: Sleep, T_A = 25°C, V_{SUP} = 14 V, ADC operation stop, WWDToperation stop, LVI operation stop			40	μA

Notes 1. This is the total current flowing to the SUP, VRO, HDS internal power supply. However, the current flow through the port pull-up resistor is not included.

2. V_{DD} current not included.

For microcontroller supply current, refer to **78K0/Kx2 User's Manual (R01UH0008E).**

LIN Transceiver Characteristics

DC Characteristics (T_A = –40 to +85°C, 6 V ≤ V_{SUP} ≤ 18 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LIN Bus dominant leak current	$I_{BUS\_PAS\_dom}$	V_{BUS} = 0 V, V_{SUP} = 12 V	–1			mA
LIN Bus recessive leak current	$I_{BUS\_PAS\_rec}$	$V_{BUS} \geq V_{SUP}$			20	μA
LIN Bus current 1	$I_{BUS\_NO\_GND}$	0 V < V_{BUS} < 18 V, V_{SUP} = 12 V	(–1)		(+1)	mA
LIN Bus current 2	I_{BUS}	V_{SUP_Device} = GND, 0 V < V_{BUS} < 18 V		(1)	(10)	μA
Receive dominant-level input voltage	V_{BUSdom}				0.4 V_{SUP}	V
Receive recessive-level Input voltage	V_{BUSrec}		0.6V_{SUP}			V
Receive centre-level threshold	V_{BUS_CNT}	$(V_{th\_dom} + V_{th\_rec})/2$	0.475V_{SUP}	0.5V_{SUP}	0.525V_{SUP}	V
<R> Receive hysteresis	V_{HYS}				0.175V_{SUP}	V
LIN dominant-level output voltage 1	$V_{BUSdom\_DRV\_LoSUP}$	V_{SUP} = 7.3 V, I_{lin} = 15 mA			1.2	V
LIN dominant-level output voltage 2	$V_{BUSdom\_DRV\_HiSUP}$	V_{SUP} = 18 V, I_{lin} = 36 mA			2	V
LIN serial diode drop voltage	$V_{SerDiode}$	V_{TxD} = V_{RO}	0.4	0.7	1.0	V
LIN pull-up resistance	R_{slave}		20	30	60	kΩ
MOD1, MOD2 high level input voltage	V_{mh}		0.7VRS			V
MOD1, MOD2 low level input voltage	V_{ml}				0.3VRS	V
SRC high level input voltage	V_{srh}		0.7VRS			V
SRC low level input voltage	V_{slrl}				0.3VRS	V
MSLP high level input voltage	V_{SLPH}		0.7VRS			V
MSLP low level input voltage	V_{SLPL}				0.3VRS	V
MSLP pull-down resistance	R_{MSLP}		50		220	kΩ
LIN thermal shutdown	LIN_{th}		(150)			°C
LIN over current limitation	I_{CONST}	LIN pin inflow current limited value	40	80	200	mA

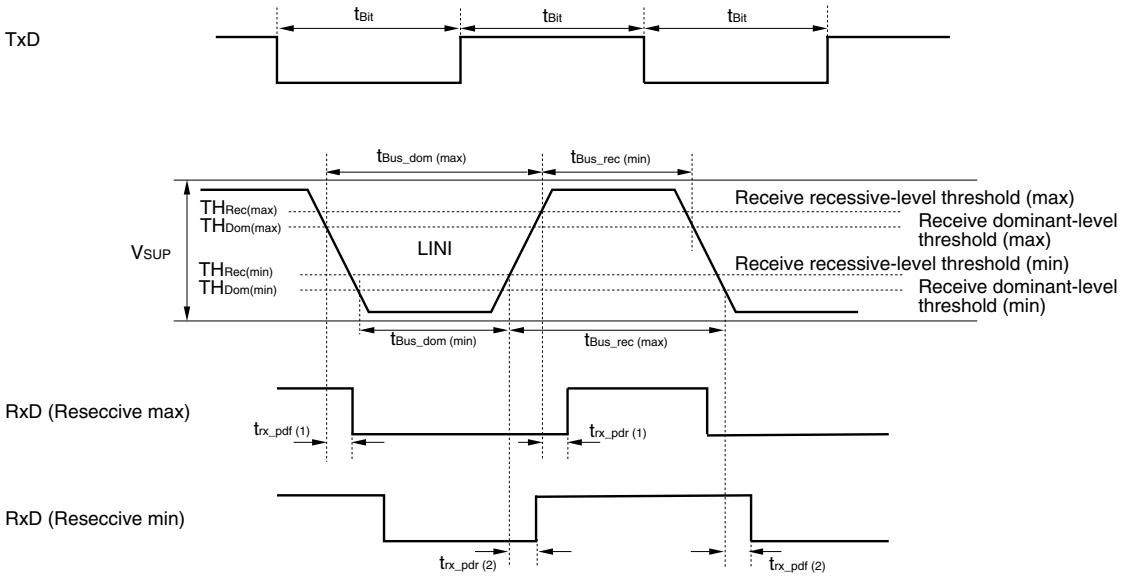
Remark The values in parentheses are based on design for which no outgoing inspection has been performed.

AC Characteristics

(T_A = –40 to +85°C, 6 V ≤ V_{SUP} ≤ 18 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Duty_Cycle1 (see figure 9-1)	D1	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 50 μs $TH_{Rec(max)}$ = 0.744×V_{SUP}, $TH_{Dom(max)}$ = 0.581×V_{SUP} D_1 = $t_{BUS\_rec(min)}$/(2×t_{BIT}) 7 V≤V_{SUP}≤18 V SRC = High	0.396			–
Duty_Cycle2 (see figure 9-1)	D2	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 50 μs $TH_{Rec(min)}$ = 0.422×V_{SUP}, $TH_{Dom(min)}$ = 0.284×V_{SUP} D_2 = $t_{BUS\_rec(max)}$/(2×t_{BIT}) 7.6 V≤V_{SUP}≤18 V SRC = High			0.581	–
Duty_Cycle3 (see figure 9-1)	D3	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 96 μs $TH_{Rec(max)}$ = 0.778×V_{SUP}, $TH_{Dom(max)}$ = 0.616×V_{SUP} D_3 = $t_{BUS\_rec(min)}$/(2×t_{BIT}) 7 V≤V_{SUP}≤18 V SRC = Low	0.417			–
Duty_Cycle4 (see figure 9-1)	D4	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 96 μs $TH_{Rec(min)}$ = 0.389×V_{SUP}, $TH_{Dom(min)}$ = 0.251×V_{SUP} D_3 = $t_{BUS\_rec(max)}$/(2×t_{BIT}) 7.6 V≤V_{SUP}≤18 V SRC = Low			0.590	–
Propagation delay	t_{rx_pd}	$t_{rx\_pdf\ (1)}$, $t_{rx\_pdf\ (2)}$, $t_{rx\_pdr\ (1)}$, $t_{rx\_pdr\ (2)}$			6	μs
LIN rising and falling transmitter delay symmetry	t_{rx_sym}	t_{rx_sym} = $t_{rx\_pdf\ (2)}$ –$t_{rx\_pdr\ (2)}$, t_{rx_sym} = $t_{rx\_pdf\ (2)}$ –$t_{rx\_pdr\ (2)}$	–2		2	μs

Figure 9-1. Duty Cycle



High-side Driver Circuit Characteristics

(T_A = −40 to +85°C, 6 V ≤ (V_{SUP} = HDS) ≤ 19 V)

Parameter	symbol	conditions	MIN.	TYP.	MAX.	UNit
Ron	$HDR_{\_RON1}$	HDR, I_O = 20 mA		50	100	Ω
HDC pull down resistance	R_{HDC}	HDC	50		220	kΩ
HDC high level input voltage	V_{IH_HDC}	HDC, I_O = −3 mA	0.7VRS		VRS	V
HDC low level input voltage	V_{IL_HDC}	HDC, I_O = 3 mA	0		0.3VRS	V
High level input leak current Note	I_{LIH1}	HDC, V_I = 5 V, Port mode A			105	μA
	I_{LIH2}	HDC, V_I = 5 V, Port mode B, C			3	μA
Low level input leak current	I_{LIL}	HDC, V_I = 0 V, Port mode A, B, C	−3			μA
Output off leak current	I_{OH1}	HDC			10	μA

Note Including the current flowing into the Pull down resistance.

High Voltage Switch Input Circuit Characteristics

(T_A = −40 to +85°C, 6 V ≤ V_{SUP} ≤ 19 V)

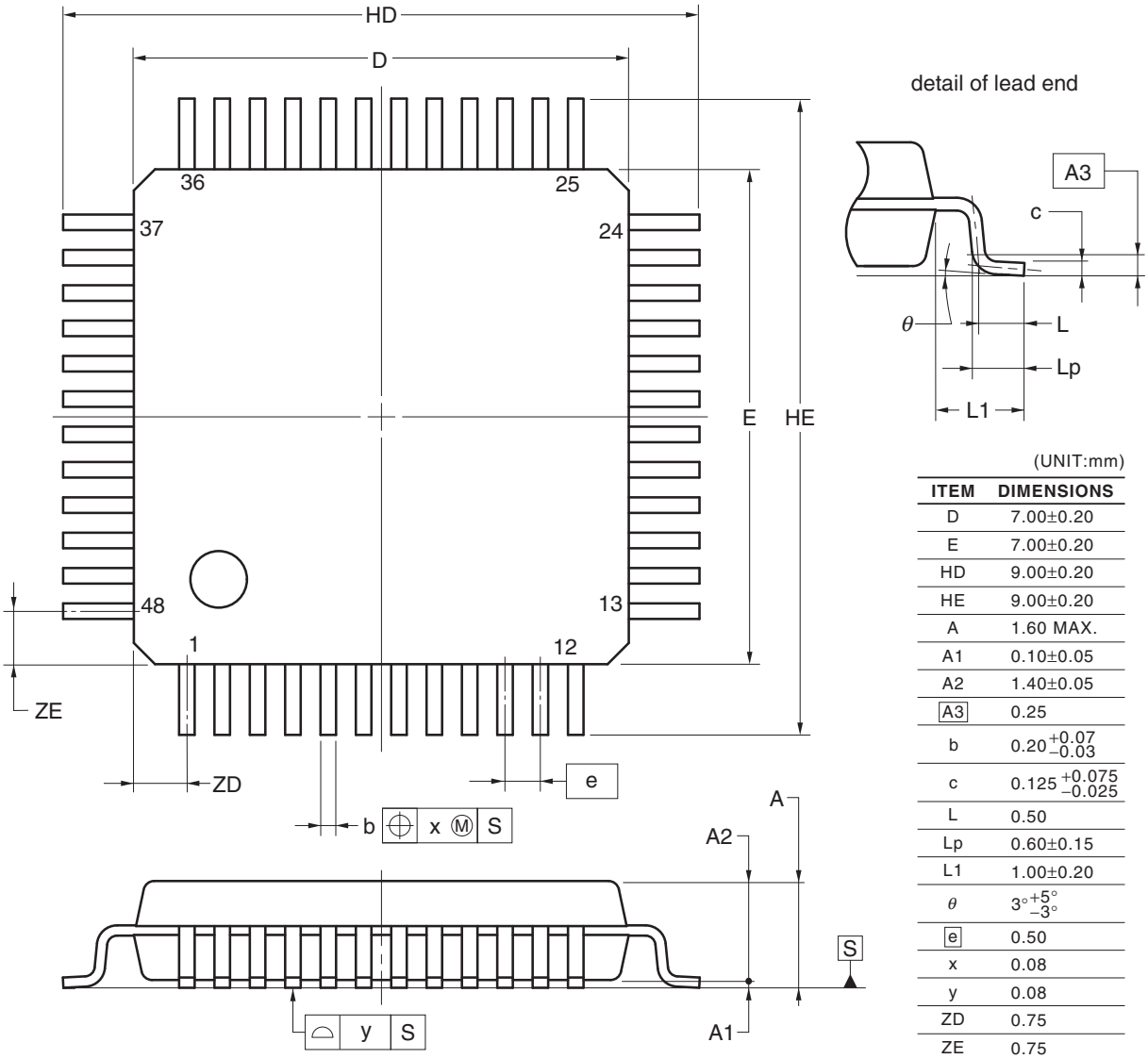
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IHW1}	SWI	0.7V_{SUP}		V_{SUP}	V
Low level input voltage	V_{ILW1}	SWI	0		0.3V_{SUP}	V
High level output voltage	V_{OHW}	SWO, I_{OH} = −3 mA	VRS−0.7			V
Low level output voltage	V_{OLW}	SWO, I_{OL} = 3 mA			0.7	V
High level input leak current	I_{LIHW1}	SWI, V_I = V_{SUP}			3	μA
Low level input leak current	I_{LILW1}	SWI, V_I = GND	−3			μA

CHAPTER 10 PACKAGE DRAWING

<R> 10.1 48 Pin Products

- μPD78F8026GAA-GAM-G, 78F8027GAA-GAM-G, 78F8028GAA-GAM-G, 78F8029GAA-GAM-G, 78F8030GAA-GAM-G, 78F8032DGA-GAM-G

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-B	P48GA-50-GAM-2	0.16



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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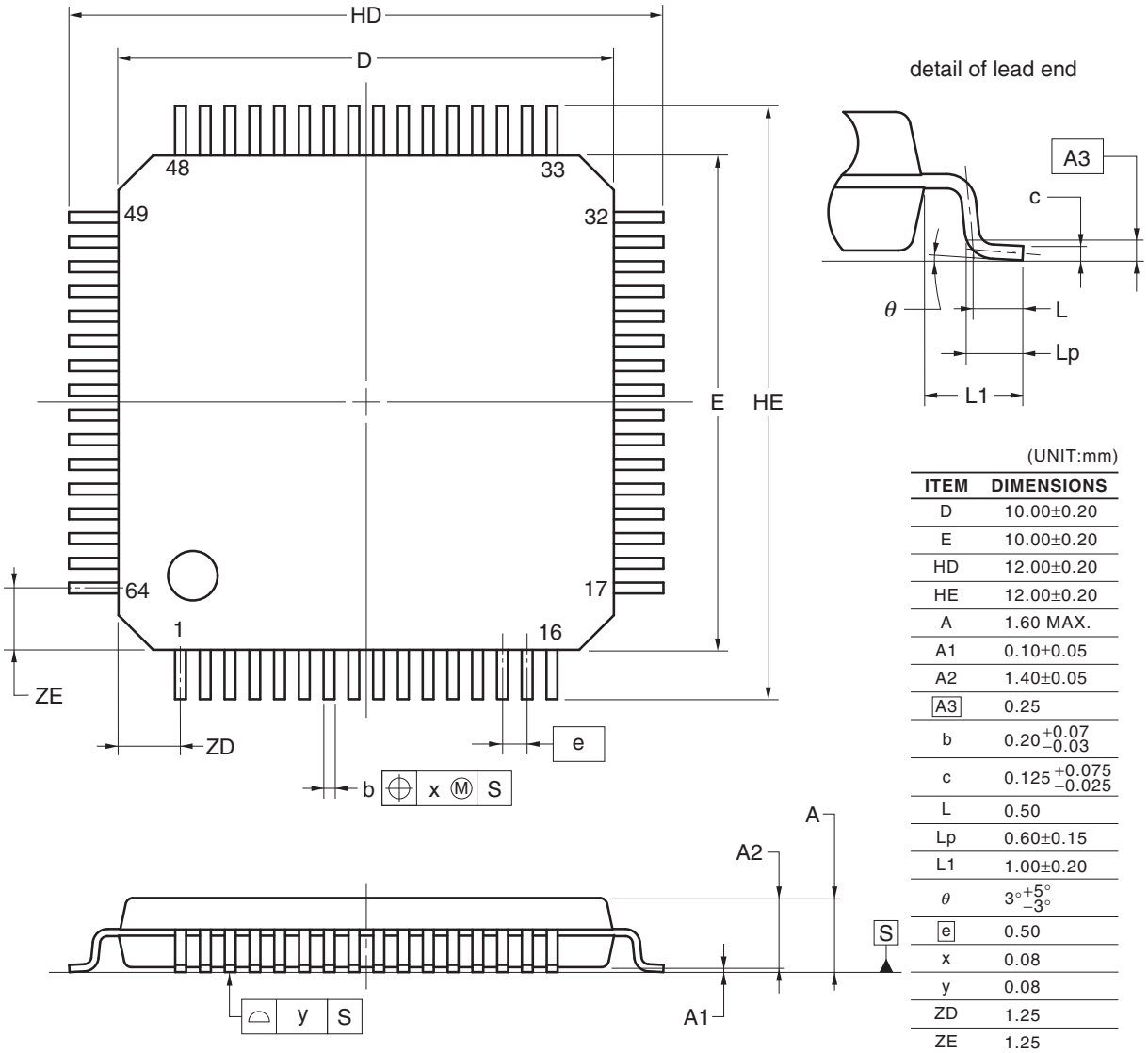
<R> 10.2 64 Pin Products

- μPD78F8033GBA-GAH-G, 78F8034GBA-GAH-G, 78F8035GBA-GAH-G, 78F8036GBA-GAH-G, 78F8037GBA-GAH-G, 78F8039DGB-GAH-G

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-B	P64GB-50-GAH-2	0.33



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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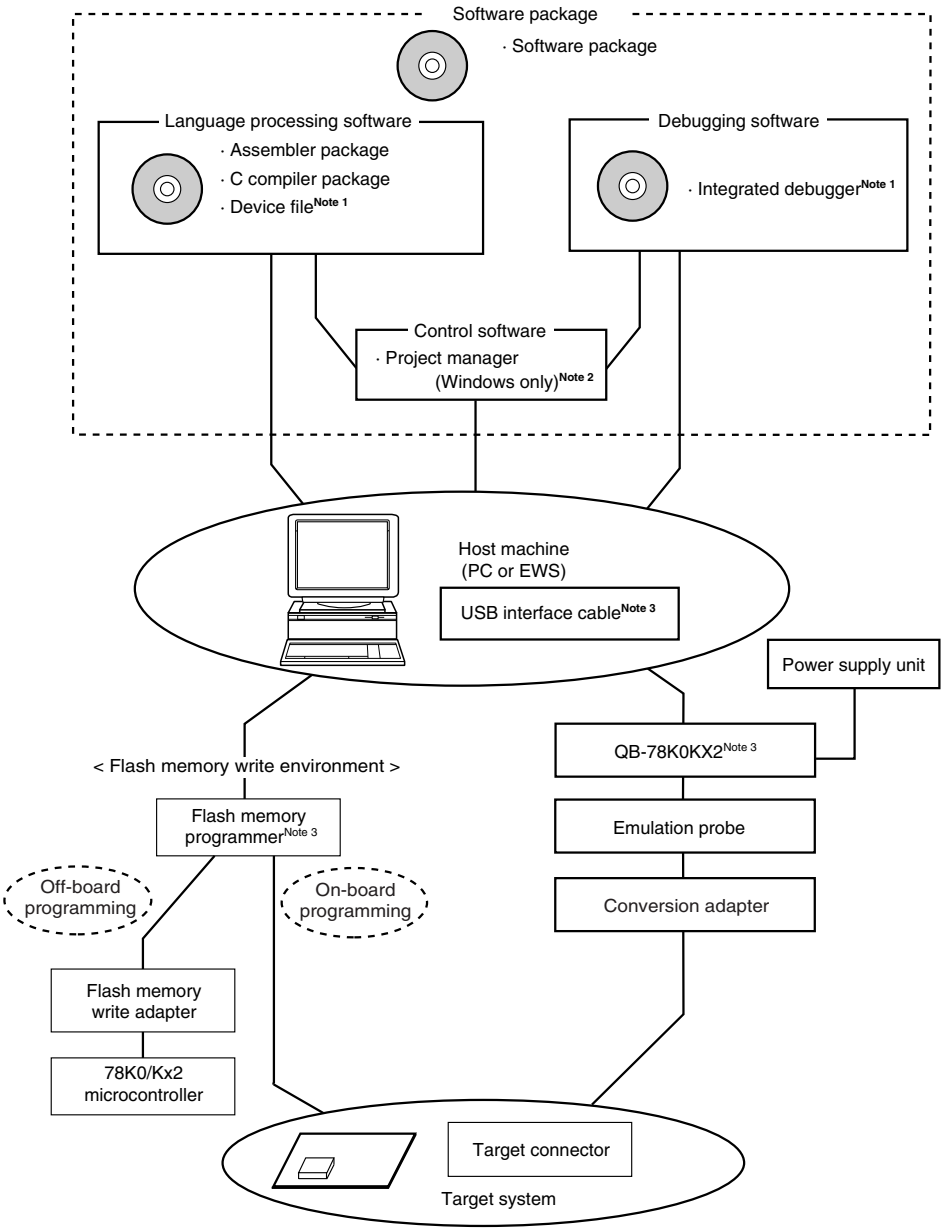
APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μPD78F802x, 78F803x microcontrollers.

Figure A-1 shows the development tool configuration.

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0KX2



<R> **Notes 1.** Download the device file for μPD78F802x, 78F803x microcontrollers and the integrated debugger ID78K0-QB from the download site for development tools.

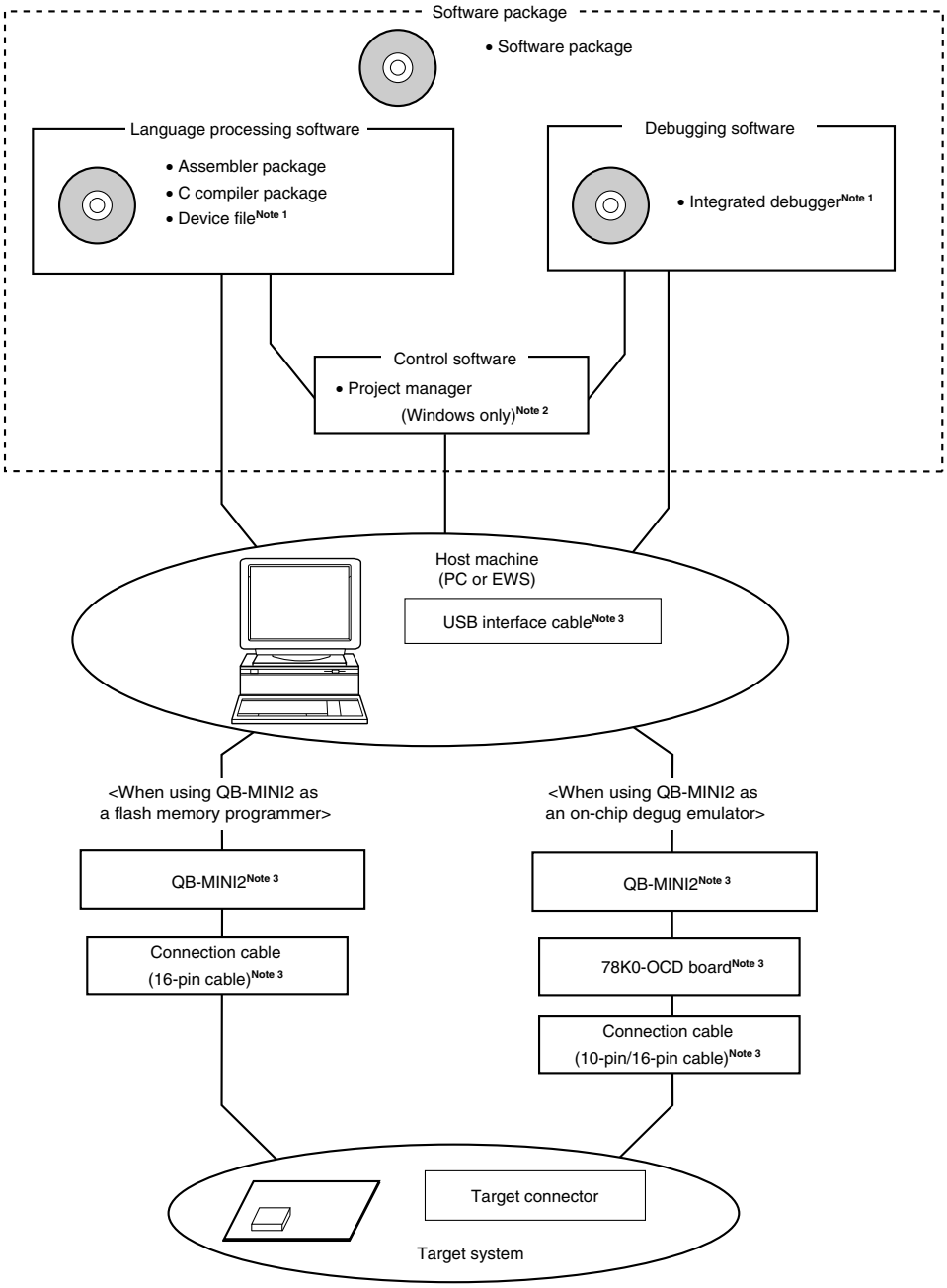
<R> (https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en)

2. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows™.

3. QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator with programming function QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.

Figure A-1. Development Tool Configuration (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



<R> **Notes 1.** Download the device file for μPD78F802x, 78F803x microcontrollers and the integrated debugger ID78K0-QB from the download site for development tools.

<R> (https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en)

2. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows.

3. QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for development tools

<R> **(**https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en)

A.1 Software Package

SP78K0 78K0 microcontroller software package	Development tools (software) common to the 78K0 microcontrollers are combined in this package.

A.2 Language Processing Software

RA78K0 Note 1 Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF788020). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
CC78K0 Note 1 C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file. **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
<R> Device file Note 2	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, ID78K0-QB, and the system simulator). The corresponding OS and host machine differ depending on the tool to be used.

Notes 1. If the versions of RA78K0 and CC78K0 are Ver.4.00 or later, different versions of RA78K0 and CC78K0 can be installed on the same machine.

2. Device file can be used in common with the RA78K0, CC78K0, ID78K0-QB, and the system simulator

A.3 Flash Memory Programming Tools

A.3.1 When using flash memory programmer FG-FP5, FL-PR5

FG-FP5, FL-PR5 Flash memory programmer	Flash memory programmer dedicated to microcontrollers with on-chip flash memory.
<R> FA-78F8039GB-GAH-RX <R> FA-78F8032GA-GAM-RX Flash memory programming adapter	Flash memory programming adapter used connected to the flash memory programmer for use. FA-78F8039GB-GAH-RX: 64-pin plastic LQFP FA-78F8032GA-GAM-RX: 48-pin plastic LQFP

Remarks 1. FL-PR5 is product of Naito Densei Machida Mfg. Co., Ltd (http://www.ndk-m.co.jp/, TEL: +81-42-750-4172).

2. Use the latest version of the flash memory programming adapter.

A.3.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers with on-chip flash memory. It is available also as on-chip debug emulator which serves to debug hardware and software when developing application systems using the 78K0/Kx2 microcontrollers. When using this as flash memory programmer, it should be used in combination with a connection cable (16-pin cable) and a USB interface cable that is used to connect the host machine.
Target connector specifications	16-pin general-purpose connector (2.54 mm pitch)

Remarks 1. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.

2. Download the software for operating the QB-MINI2 from the download site for development tools.
<R> **(**https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en)

A.4 Debugging Tools (Hardware)

A.4.1 When using in-circuit emulator QB-78K0KX2

QB-78K0KX2 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2 microcontrollers. It supports to the integrated debugger (ID78K0-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
<R> QB-78F8039-EA-01T <R> QB-78F8032-EA-01T Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector. Exchange adapter has the LIN transceiver, voltage regulator and driver functions. QB-78F8039-EA-01T: 64-pin plastic LQFP QB-78F8032-EA-01T: 48-pin plastic LQFP
<R> QB-64GB-YS-01T <R> QB-48GA-YS-01T Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator. QB-64GB-YS-01T: 64-pin plastic LQFP QB-48GA-YS-01T: 48-pin plastic LQFP
QB-64GB-YQ-01T, QB-48GA-YQ-01T YQ connector	This YQ connector is used to connect the target connector and exchange adapter. QB-64GB-YQ-01T: 64-pin plastic LQFP QB-48GA-YQ-01T: 48-pin plastic LQFP
QB-64GB-HQ-01T, QB-48GA-HQ-01T Mount adapter	This mount adapter is used to mount the target device with socket. QB-64GB-HQ-01T: 64-pin plastic LQFP QB-48GA-HQ-01T: 48-pin plastic LQFP
QB-64GB-NQ-01T, QB-48GA-NQ-01T Target connector	This target connector is used to mount on the target system. QB-64GB-NQ-01T: 64-pin plastic LQFP QB-48GA-NQ-01T: 48-pin plastic LQFP

Remark The QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Download the software for operating the QB-MINI2 from the download site for development tools.

<R> (https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en)

A.4.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. When using this as on-chip debug emulator, it should be used in combination with a connection cable (10-pin cable or 16-pin cable), a USB interface cable that is used to connect the host machine, and the 78K0-OCD board.
Target connector specifications	10-pin general-purpose connector (2.54 mm pitch) or 16-pin general-purpose connector (2.54 mm pitch)

Remarks 1. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.

2. Download the software for operating the QB-MINI2 from the download site for development tools. <R> (https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en)

A.5 Debugging Tools (Software)

ID78K0-QB Note Integrated debugger	This debugger supports the in-circuit emulators for the 78K0 microcontrollers. The ID78K0-QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file.

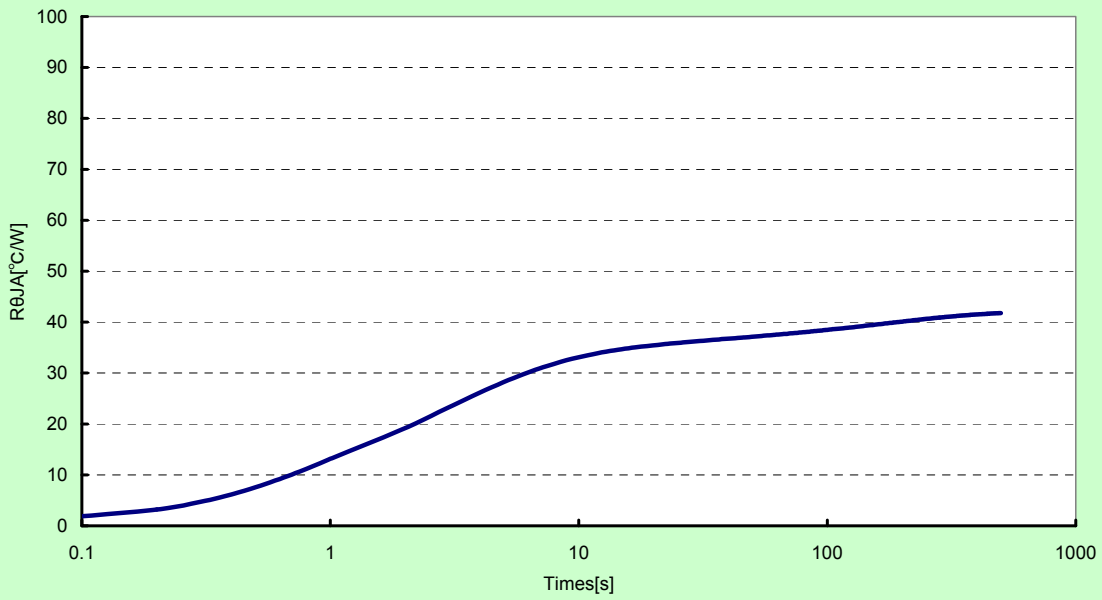
Note Download the ID78K0-QB from the download site for development tools <R> (https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en).

APPENDIX B QFP PACKAGE THERMAL RESISTANCE

<R> **Condition 1**

Package:	48-pin plastic LQFP
Substrate size:	76.2 x 114.3 mm, t = 1.6 mm
Trace layer:	Four-layer (thickness of trace: 70/35/35/70 μm)
Material:	FR-4

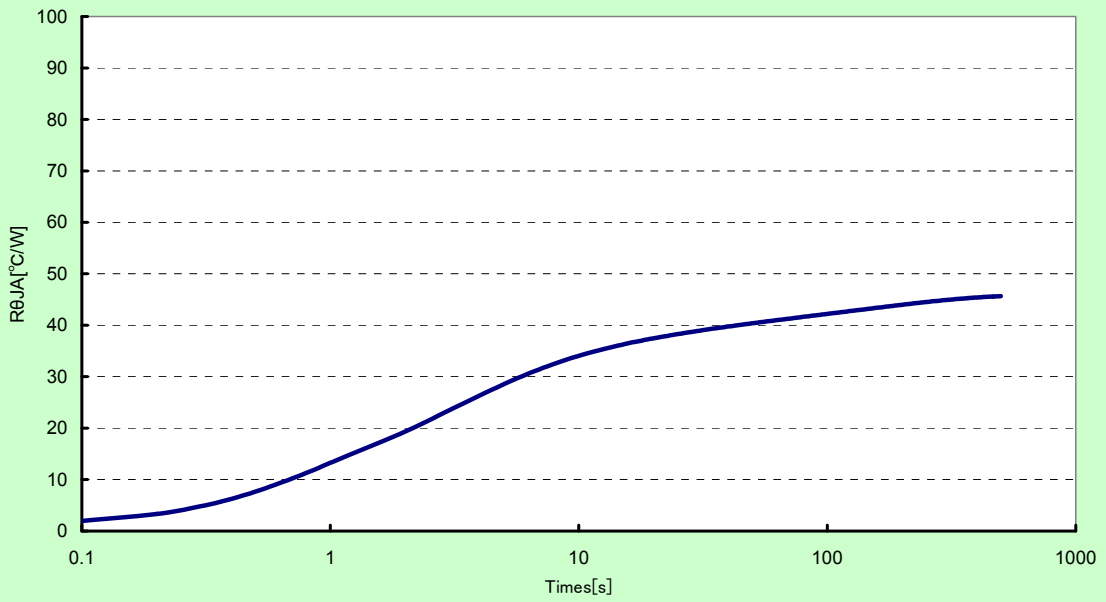
Package thermal resistance(Typ.)



<R> **Condition 2**

Package:	48-pin plastic LQFP
Substrate size:	76.2 x 114.3 mm, t = 1.6 mm
Trace layer:	Two-layer (thickness of trace: 70/-/-/70 μm)
Material:	FR-4

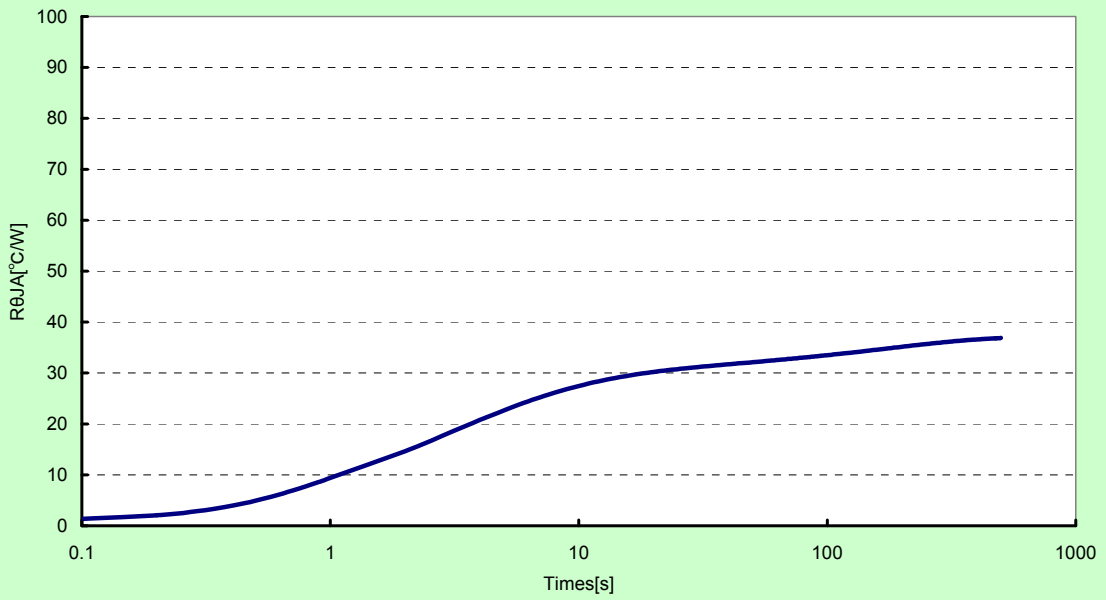
Package thermal resistance(Typ.)



<R> **Condition 3**

Package:	64-pin plastic LQFP
Substrate size:	76.2 x 114.3 mm, t = 1.6 mm
Trace layer:	Four-layer (thickness of trace: 70/35/35/70 μm)
Material:	FR-4

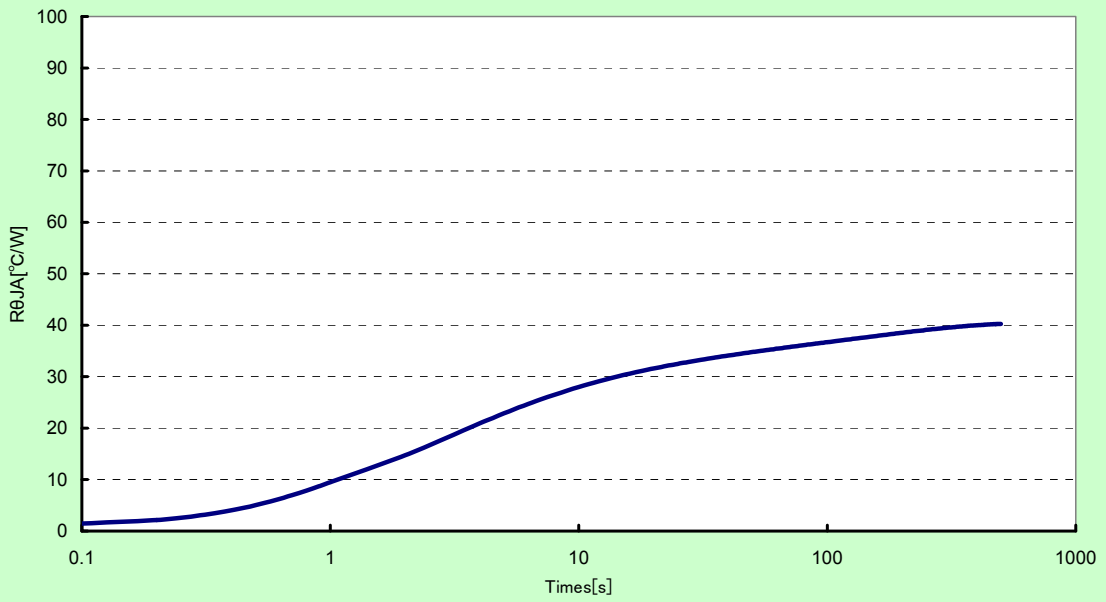
Package thermal resistance(Typ.)



<R> **Condition 4**

Package:	64-pin plastic LQFP
Substrate size:	76.2 x 114.3 mm, t = 1.6 mm
Trace layer:	Two-layer (thickness of trace: 70/-/-/70 μm)
Material:	FR-4

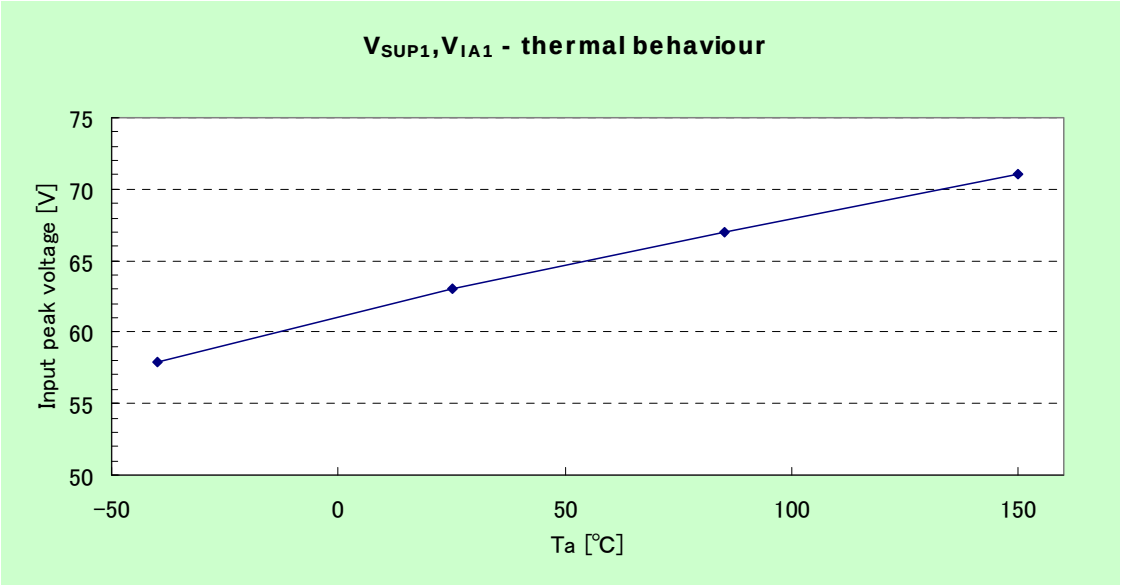
Package thermal resistance(Typ.)



APPENDIX C THERMAL BEHAVIOUR OF ABSOLUTE MAXIMUM RATINGS FOR ANALOG BLOCK

Conditions

Target parameters:	V_{SUP1}, V_{IA1}
Target pins:	V_{SUP}, HDS, LIN, SWI
Measured temperature (Ta):	–40 to +150°C
Applied voltage time:	400 ms



REVISION HISTORY

<R> Major Revisions in This Edition

(1/2)

Page	Description
Throughout	Deletion of the following devices: μPD78F8026K8A-5B4-G, μPD78F8026K8A2-5B4-G, μPD78F8027K8A-5B4-G, μPD78F8027K8A2-5B4-G, μPD78F8028K8A-5B4-G, μPD78F8028K8A2-5B4-G, μPD78F8029K8A-5B4-G, μPD78F8029K8A2-5B4-G, μPD78F8030K8A-5B4-G, μPD78F8030K8A2-5B4-G, μPD78F8032DK8-5B4-G Update of URL.
p. 2	**1.1 Features** Change of description of LIN transceiver, Package, and Operating ambient temperature
p. 3	**1.3 Ordering Information** Deletion of 48-pin plastic WQFN (fine pitch) (7×7) devices
p. 4, 5	**1.4 Pin Configuration (Top View)** Deletion of 48-pin plastic WQFN (fine pitch) (7×7) Change of **Cautions**
p. 8	**1.5 Block Diagram** Modification of I/O direction at MOD1 pin of μPD78F8033 to 78F8037, 78F8039D
pp. 12, 13, 15	**1.6 Outline of Functions** • μPD78F8026 to 78F8030, 78F8032D Deletion of description about (A2) grade products from Power supply voltage Deletion of T_A = −40 to +125°C from Operating ambient temperature Deletion of description about SAE-J2602 compliance from LIN transceiver • μPD78F8033 to 78F8037, 78F8039D Deletion of description about SAE-J2602 compliance from LIN transceiver
pp. 18, 19	**2.3.1 (2) Non-port functions: μPD78F8026 to 78F8030, 78F8032D** Change of description in Function for the following pins: SI10, SO10, SDA0, $\overline{SCK10}$, SCL0, RxD0, RxD6, TxD0, TxD6, REGC, V_{DD}, V_{SS} Change of I/O of the following pins: AV_{REF}, X1
pp. 21, 22	**2.3.2 (2) Non-port functions: μPD78F8033 to 78F8037, 78F8039D** Change of description in Function for the following pins: SI10, SO10, SDA0, $\overline{SCK10}$, SCL0, RxD0, RxD6, TxD0, TxD6, REGC, V_{DD}, V_{SS} Change of I/O of the following pins: AV_{REF}, X1, XT1
p. 33	**2.5.13 REGC** Change of description
p. 36	**Table 2-3 Pin I/O Circuit Types** Addition of **Note 3** to FLMD0 pin Change of description of AV_{REF} and AV_{SS} pins Addition of description of REGC pin
p. 43	**Table 4-1 Wiring of Dedicated Flash Programmer** Modification of pin number of MSLP pin for 64-pin package
p. 44	**5.3 Power Supply Thermal Shutdown Function** Addition of description to **Caution**

Page	Description
p. 46	**6.1 LIN Transceiver Function** Change of description
p. 51	**6.4 Thermal Shutdown Circuit** Addition of description to **Caution**
p. 54	**CHAPTER 9 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)** Deletion of **Caution 1**
p. 55	**CHAPTER 9 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS) (2) Non-port functions** Addition of UART0 to table
pp. 56 to 78	Modification of caution number to be referred
p. 58	**9.1 Absolute Maximum Ratings for Analog Block (T_A = 25°C)** Change of ratings of output currents I_{HDR} and I_{SWO}
p. 61	**9.2 Microcontroller Block Characteristics DC Characteristics (1/4)** Change of values in calculation example of **Note 3**
p. 64	**9.2 Microcontroller Block Characteristics DC Characteristics (4/4)** Change of condition of supply currents I_{DD1}, I_{DD2}, and I_{DD3} Addition of condition to A/D converter operating current (I_{ACC})
p. 66	**9.2 Microcontroller Block Characteristics AC Characteristics (1) Basic operation (1/2)** Change of conditions for peripheral hardware clock frequency f_{PRS}
p. 79	**9.3 Analog Block Characteristics Voltage regulator circuit characteristics** Change of condition for V_{CCOUT3}
p. 80	**9.3 Analog Block Characteristics LIN Transceiver Characteristics DC Characteristics** Change of maximum value of receive hysteresis
–	Deletion of the following chapters **CHAPTER 10 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: TA = –40 to +110°C)) (TARGET)** **CHAPTER 11 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: TA = –40 to +125°C)) (TARGET)**
pp. 84, 85	Change of package drawings in **10.1 48 Pin Products** and **10.2 64 Pin Products** Deletion of package drawing of 48-pin plastic WQFN (7×7)
pp. 87, 88	**Figure A-1 Development Tool Configuration** **(1) When using the in-circuit emulator QB-78K0KX2** **(2) When using the on-chip debug emulator with programming function QB-MINI2** Change of description of **Note 1**
p. 89	**A.2 Language Processing Software** Deletion of “(under development)” from Device file
p. 90	**A.3.1 When using flash memory programmer FG-FP5, FL-PR5** Addition of produce names to Flash memory programming adapter Deletion of “(under development)”
p.91	**A.4.1 When using in-circuit emulator QB-78K0KX2** Addition of produce names to Exchange adapter (under development) and Space adapter (under development) Deletion of “(under development)”
pp. 93 to 96	**APPENDIX B PACKAGE THERMAL RESISTANCE** Change of **Conditions 1** and **2** Addition of **Conditions 3** and **4**

<R> Revision History of Preceding Edition

Here is the revision history of the preceding edition. Chapter indicates the chapter of the preceding edition.

Edition	Description	Chapter
0.02	Change of **1.6 Outline of Functions**	**CHAPTER 1 OUTLINE**
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μPD78F802x, 78F803x Microcontrollers
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