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ISL6420BEVAL7Z - User Guide

Introduction

The ISL6420BEVAL7Z is a negative buck boost converter, which features the ISL6420B PWM controller.

The ISL6420B is a wide input range, synchronous buck controller. It is designed to drive N-Channel MOSFETs in a synchronous rectified buck topology for up to 25A load current. The ISL6420B integrates control, output adjustment, monitoring and protection functions into a single package. The ISL6420BEVAL7Z is configured with the ISL6420B in an inverting buck/boost topology. The output voltage is set at 5V. At 12V input, the maximum load current is 25A. All the necessary components are with 2.2"x 1.25" PCB area.

The ISL6420B provides simple, voltage mode control with fast transient response. The operating frequency can be adjustable from 100kHz to 1.4MHz.

The ISL6420B is offered in a space saving 4x4 QFN and easy-to-use 20 Ld QSOP package.

When used in an inverting buck/boost converter, the ISL6420B sees the V_{IN} + V_{OUT} and the inductor current as higher than the load current.

FIGURE 1. ISL6420BEVAL7Z TOP VIEW (ONE-SIDE PLACEMENT)

Evaluation Board Specifications

TABLE 1. BOARD ELECTRICAL SPECIFICATIONS

SPEC	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
V_{IN}	Input Voltage	5		16	V
V_{OUT}	Output Voltage, 0A < I_{OUT} <20A	-4.75	-5.0	-5.25	V
I_{OUT}	Maximum Load Current, V_{IN} > 10V		20		A
F_{SW}	Switching Frequency		280		kHz
η	Efficiency, V_{IN} = 12V, I_{OUT} = 20A		93		%

Recommended Equipment

The following equipment is recommended for evaluation:

- 0V to 20V power supply with 20A source current capability
- Electronic load capable of sinking 25A
- Digital Multimeters (DMMs)
- 100MHz Quad-Trace Oscilloscope

Controller Key Features

- Wide V_{IN} Range
  - 5.6V to 28V
  - 4.5V to 5.5V
- Resistor-Selectable Switching Frequency from 100kHz to 1.4MHz
- Voltage Margining and External Reference Tracking Modes
- Upper MOSFET $r_{DS(ON)}$ for Current Sensing
- Support Pre biased Start-Up
- Programmable Soft-Start
- Extensive Protection Functions:
  - Overvoltage, Overcurrent, Undervoltage

TABLE 2. RECOMMENDED COMPONENT SELECTION FOR QUICK EVALUATION

V_{IN} (v)	V_{OUT} (V)	I_{OUT} (A)	UPPER MOSFET	LOWER MOSFET	INDUCTOR	F_{SW}/RT	TOTAL CERAMIC C_{IN}
12	-5	20	2X BSC057N03 LS	2X BSC057N03 LS	SER2010-901ML	300kHz/52.3kΩ	4 x 10µF
12	-5	10	1X BSC057N03 LS	1X BSC030N03 LS	SER2009-901ML	500kHz/31.6kΩ	2 x 10µF

Please contact Intersil Sales for assistance.

Quick Test Setup

1. Ensure that the Evaluation board is correctly connecting to the power supply and the electronic load prior to applying any power. Please refer to Figure 2 for proper set-up.
2. Connect jumpers J1, J2, J3 and J8 in the positions specified in Table 3.
3. Turn on the power supply, V_{IN} < 16V.
4. Adjust input voltage V_{IN} within the specified range and observe output voltage. The output voltage variation should be within 5%.
5. Adjust load current within 20A. The output voltage variation should be within 5%.
6. Use oscilloscope to observe output ripple voltage and phase node ringing. For accurate measurement, please refer to Figure 3 for proper probe set-up.
7. Optimization. Please refer to Table 2 on page 1 for optimization recommendation.

NOTE: Test points: P3, 4, 5, 6 (GND, V_{OUT}, GND, V_{IN}) are for voltage measurement only. Do not allow high current through these test points.

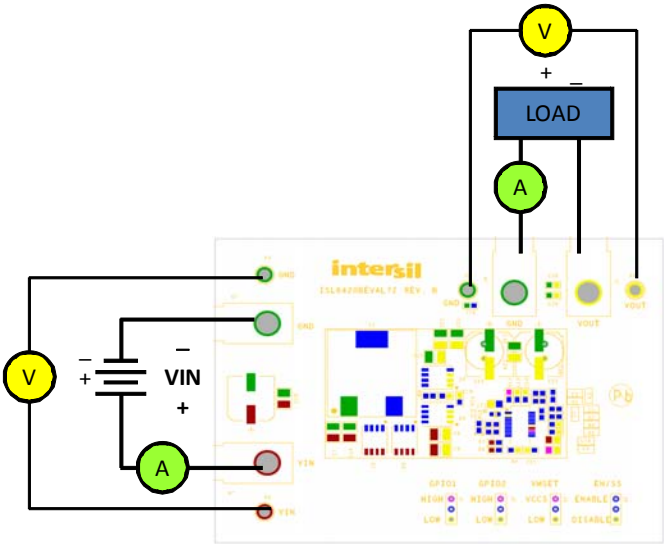

FIGURE 2. ISL6420BEVAL7Z TEST SET-UP

TABLE 3. JUMPER POSITION

	J1/GPIO1	J2/GPIO2	J3/VMSET	J8/EN/SS
SHUTDOWN	LOW	LOW	DOES NOT MATTER	DISABLE
NORMAL	LOW	LOW	VCC5	ENABLE
Margining Up	LOW	HIGH	OPEN/R_{12} set ΔVO	ENABLE
Margining Down	HIGH	LOW	OPEN/R_{12} set ΔVO	ENABLE

Probe Set-up

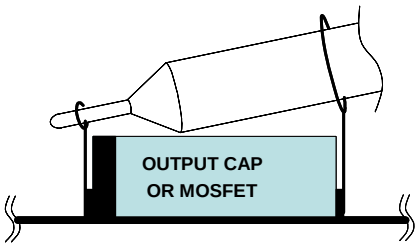

FIGURE 3. OSCILLOSCOPE PROBE SET-UP

Evaluation Board Usage

Component Voltage Stress

The controller, ISL6420B, MOSFETs and the ceramic input capacitors are connected from the V_{IN} rail to the V_{OUT} rail. Thus, these components see a voltage stress of the sum of V_{IN} and V_{OUT}.

Setting V_{OUT}

The output voltage is set by the resistor divider, R_4 and R_1.

$$V_{OUT} = \frac{R_1 + R_4}{R_4} \times 0.6V \quad \text{(EQ. 1)}$$

Duty Cycle Calculation

The duty cycle of the inverting buck/boost converter can be calculated by Equation 2:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \quad \text{(EQ. 2)}$$

Component Selection

Inductor

The inductor is selected by the DC current, saturation current and overall thermal performance.

The inductor DC current can be calculated by Equation 3:

$$I_{LDC} = \frac{I_{OUT}}{1 - D} \quad \text{(EQ. 3)}$$

Maximum DC current occurs at minimum input with Equation 4:

$$I_{LDCmax} = I_{OUT} \times \frac{V_{inmin} + V_{OUT}}{V_{inmin}} \quad \text{(EQ. 4)}$$

Inductor core loss is related to the switching frequency and the inductor ripple current. Please refer to Equation 5 for inductor ripple estimation

$$\Delta i_{P-P} = \frac{(1 - D) \times V_{OUT}}{L \times F_{SW}} \quad \text{(EQ. 5)}$$

Inductor vendors provide formula and/or design tools for core loss estimation. Please refer to the inductor datasheet for thermal stress estimation.

The peak inductor current is as shown with Equation 6:

$$I_{LPK} = I_{LDCmax} + \frac{\Delta i_{P-P}}{2} \quad \text{(EQ. 6)}$$

Please select inductor with saturation current higher than the maximum peak inductor current.

For overcurrent protection setting, please set IOC higher than the maximum peak current and refer to the ISL6420B datasheet, FN6901 for details.

Input Capacitors

The input capacitors can be connected from V_{IN} to GND, e.g. C_7, C_{14} and C_{18}, or from V_{IN} to V_{OUT}, e.g. C_8 and C_9. Several trade-offs need to be considered regarding the arrangement of the input capacitors.

It is generally recommended that bulk input capacitors (which are usually of the aluminum electrolytic type), be connected from V_{IN} to GND, C_{18} with small ceramic capacitors, Cin_ce (C_7 and C_{14}, as shown in the schematic in parallel). These capacitors are for lowering the input power supply impedance, thus stabilizing the overall system.

Ceramic capacitors, CF (C_8 and C_9, as shown in the schematic) are connected from V_{IN} to V_{OUT} for ripple current filtering. C_8 and C_9 should be rated above the sum of V_{OUT} and V_{IN}.

The total input RMS current can be estimated with Equation 7:

$$I_{INRMS} = I_O \times \sqrt{\frac{D}{1-D} + \frac{(\Delta i_{P-P})^2}{12}(D)} \quad \text{(EQ. 7)}$$

Where Δi_{P-P} is the inductor peak-to-peak ripple.

Worst case for input RMS current is at minimum V_{IN}.

The rule of thumb is that the input ripple current be shared by all the input ceramic capacitors, C_7, C_{14}, C_8 and C_9.

From the output ripple perspective, is preferred to place all capacitors from V_{IN} to V_{OUT}. In some applications, the voltage across V_{IN} and V_{OUT} is so high, that the cost of the high voltage ceramic capacitors does not justify the benefit. However, it is required to place a small ceramic capacitor across the MOSFETs.

Output Capacitors

It is recommended to use a combination of aluminum electrolytic capacitors with high capacitance and low ESR ceramic capacitors at the output for optimum ripple and load transient performance.

The total output RMS current can be estimated with Equation 8:

$$I_{OUTRMS} = I_O \times \sqrt{\frac{D}{1-D} + \frac{(\Delta i_{P-P})^2}{12}(1-D)} \quad \text{(EQ. 8)}$$

Where Δi_{P-P} is the inductor peak-to-peak ripple.

Worst case for the total output RMS current is at minimum V_{IN} and maximum load.

The input capacitor across the MOSFETs, CF can alleviate the RMS current through the output capacitors.

Accurate RMS current distribution can be obtained by simulation. The rule of thumb calculation of the RMS through the output capacitors is as shown with Equation 9:

$$I_{CORMS} = I_O \times \sqrt{\frac{D}{1-D} + \frac{(\Delta i_{P-P})^2}{12}(1-D)} \times \frac{CF}{Coce + CF} \quad \text{(EQ. 9)}$$

Where Coce is the total output ceramic capacitance.

Starting with No Load

Prior to the enabling or the VCC reaching UVLO threshold, the ISL6420B draws 3mA current. This shutdown current forward bias the low-side MOSFET body diode. Thus, the output voltage is reversed with the voltage amplitude clamped at the diode-forward voltage.

If this condition is not acceptable, a dummy load can be used to bypass this shutdown current. The dummy resistor can be calculated by Equation 10:

$$R_{DUMMY} = \frac{V_{neg}}{I_{OP}} \quad \text{(EQ. 10)}$$

where, V_{neg} is the allowable negative voltage at the output. I_{OP} is the operating current by the ISL6420B, which is 3mA maximum.

Typical Performance Curves

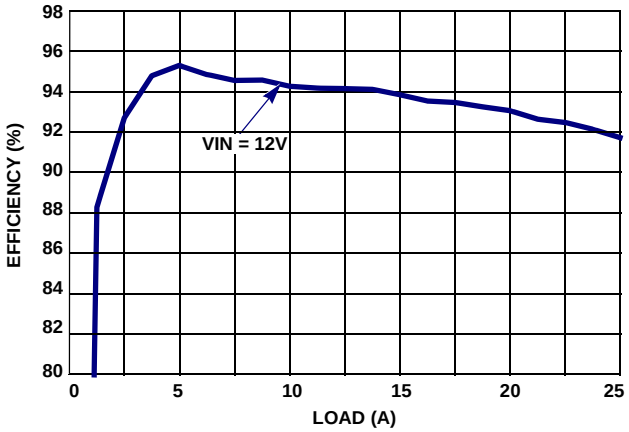

FIGURE 4. EFFICIENCY vs LOAD CURRENT (V_{IN} = 12V, REFER TO TABLE 2 FOR COMPONENTS)

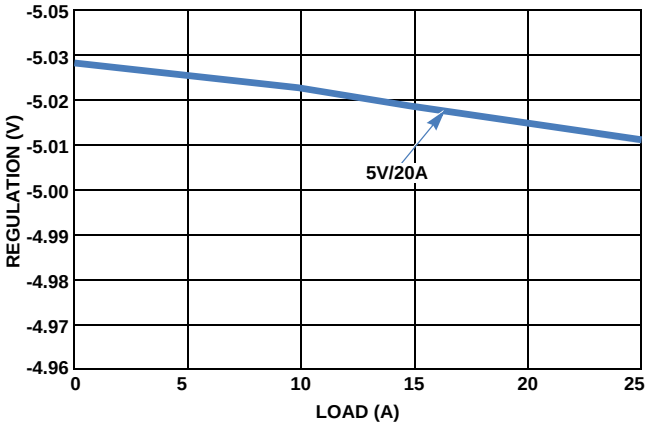

FIGURE 5. LOAD REGULATION, (V_{IN} = 12V)

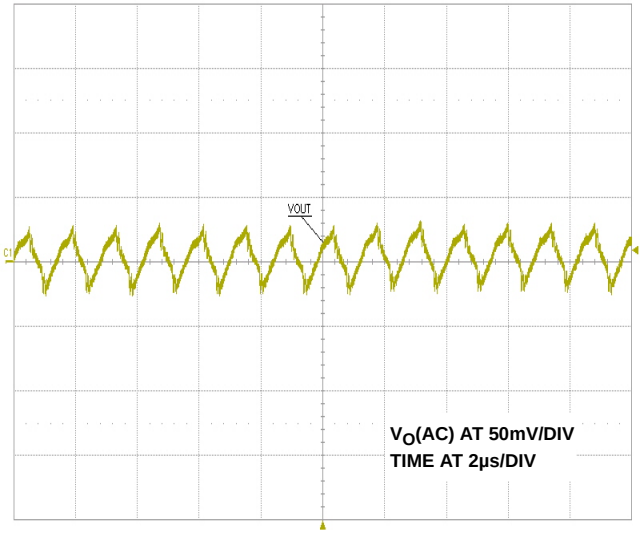

FIGURE 6. OUTPUT RIPPLE (V_{IN} = 12V, V_0 = 5V, LOAD = 0A)

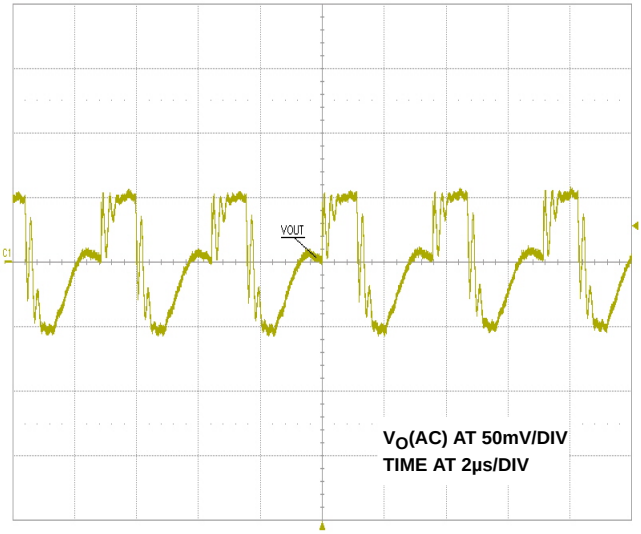

FIGURE 7. OUTPUT RIPPLE (V_{IN} = 12V, V_0 = 5V, LOAD = 20A)

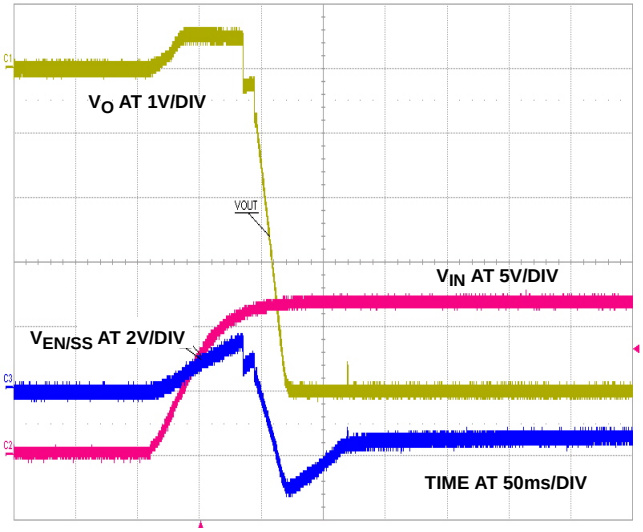

FIGURE 8. SOFT - START (C_{SS} - 0.47µF, C_{DEL} = 0.1µF, NO LOAD, All SIGNAL REFERRING TO GND)

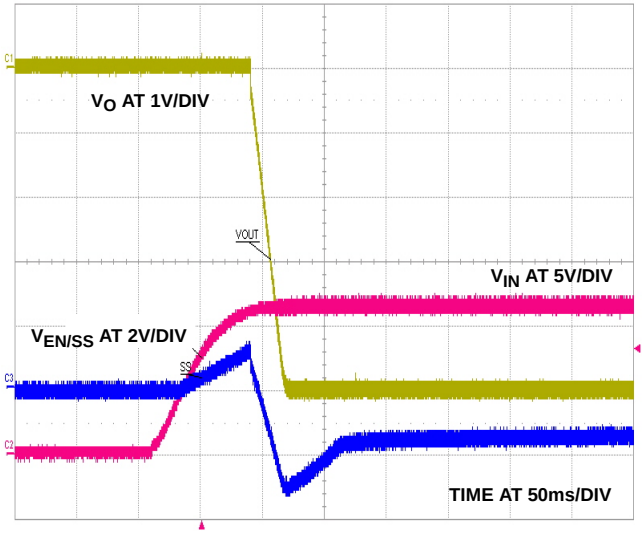

FIGURE 9. SOFT - START (C_{SS} - 0.47µF, C_{DEL} = 0.1µF, 20A LOAD, SIGNAL REFERRING TO GND)

Typical Performance Curves (Continued)

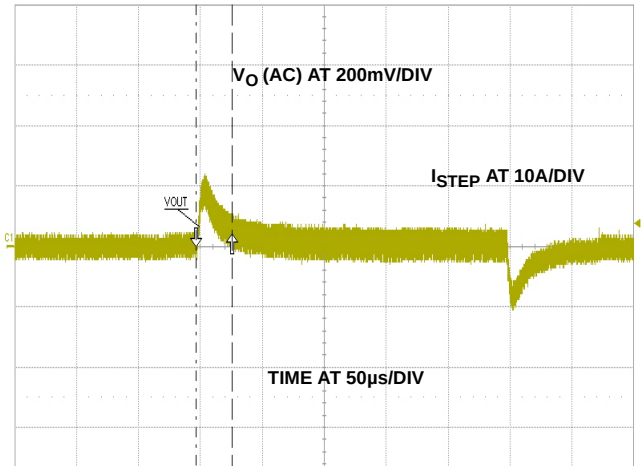

FIGURE 10. LOAD TRANSIENT (LOAD STEP FROM 5A TO 15A, di/dt = 2A/µs)

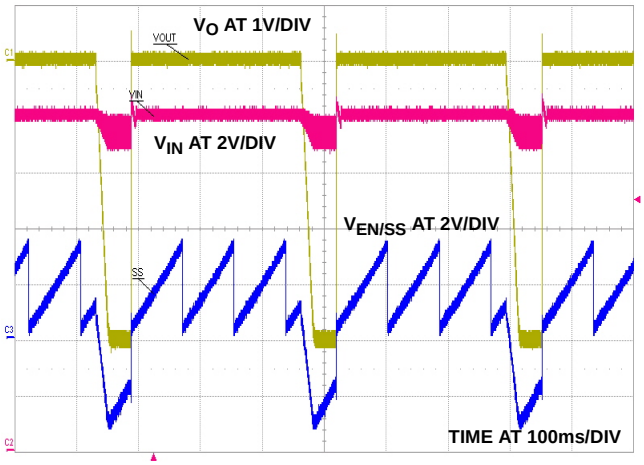

FIGURE 11. OVERCURRENT PROTECTION

ISL6402BEVAL7Z Schematic

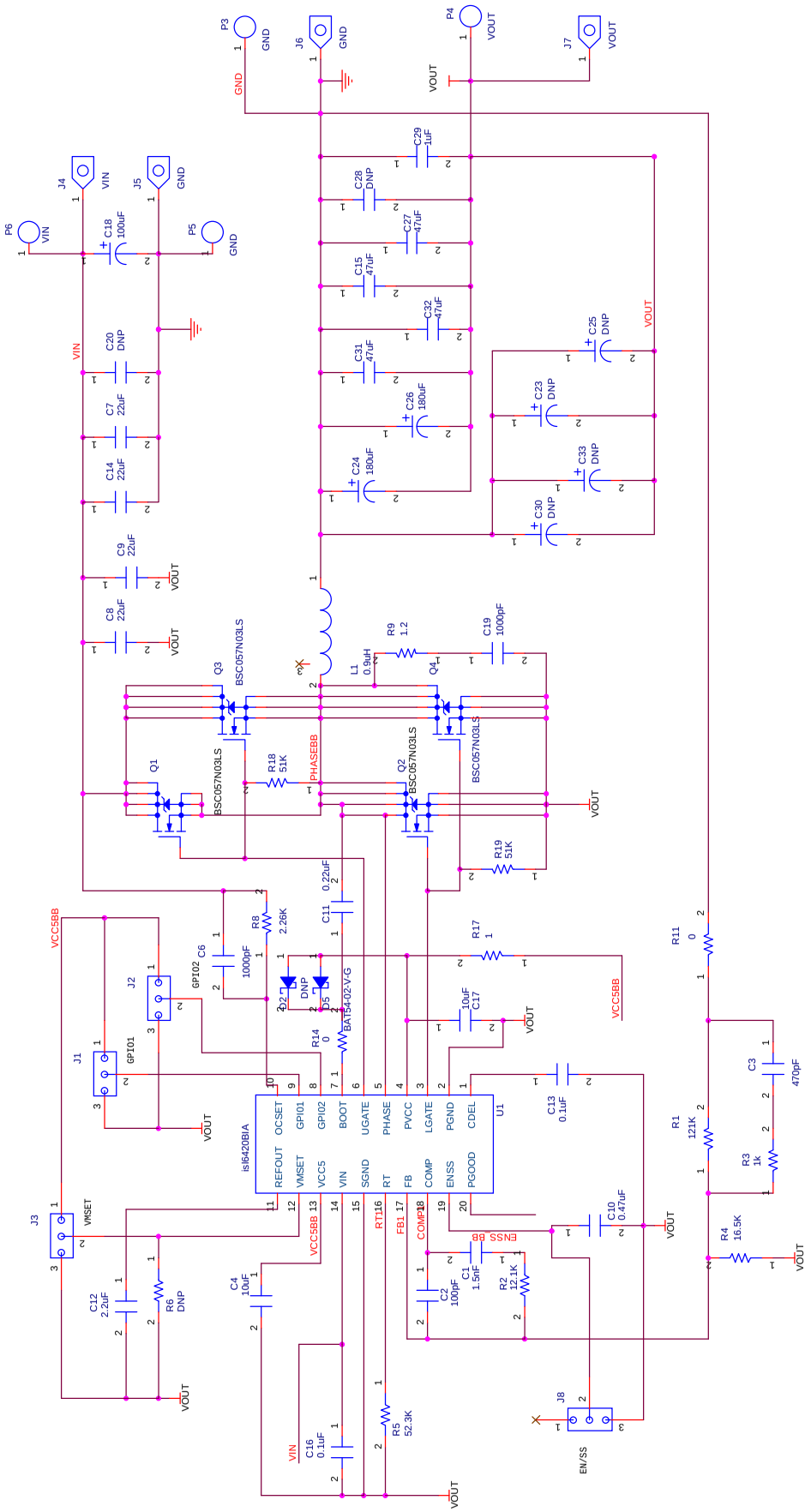

TABLE 4. BILL OF MATERIALS

ITEM	QTY	PART REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
ESSENTIAL COMPONENTS						
1	1	C1	1500pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
2	1	C2	100pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
3	1	C3	470pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
4	2	C4, C17	10µF	Ceramic CAP, X5R, 10V, sm0805	GENERIC	GENERIC
5	2	C6, C19	1000pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
6	3	C7, C8, C9, C14	22µF	Ceramic CAP, X5R , 25V, sm1210	GENERIC	GENERIC
7	1	C10	0.47µF	Ceramic CAP, X5R, 16V, sm0603	GENERIC	GENERIC
8	1	C11	0.22µF	Ceramic CAP, X5R, 16V, sm0603	GENERIC	GENERIC
9	1	C12	2.2µF	Ceramic CAP, X5R, 16V, sm0603	GENERIC	GENERIC
10	2	C13, C16	0.1µF	Ceramic CAP, X5R, 50V, sm0603	GENERIC	GENERIC
11	4	C15, C27, C31, C32	47µF	Ceramic CAP, X5R, 10V, sm1210	GENERIC	GENERIC
12	1	C18	100µF	Alum. Cap, 50V	EMVA500ADA101MHA0G	United Chemi-Con
13	2	C24, C26	180µF	OSCON, 16V, Radial 8x9	16SEPC180MX	SANYO
14	1	C29	1µF	Ceramic CAP, X5R, 25V, sm0603	GENERIC	GENERIC
15	1	D5		Schottky Diode, 30V, SOD523	BAT54-02-V-G	Vishay
16	1	L1	0.9µH	Inductor	SER2010-901ML	Coilcraft
17	4	Q1, Q2, Q3, Q4		Single Channel NFET, 30V	BSC057N03LS G	Infineon
18	1	R1	121kΩ	Resistor, sm0603, 1%	GENERIC	GENERIC
19	1	R2	12.1kΩ	Resistor, sm0603, 1%	GENERIC	GENERIC
20	1	R3	1kΩ	Resistor, sm0603, 1%	GENERIC	GENERIC
21	1	R4	16.5kΩ	Resistor, sm0603, 1%	GENERIC	GENERIC
22	1	R5	52.3kΩ	Resistor, sm0603, 1%	GENERIC	GENERIC
23	1	R8	2.26kΩ	Resistor, sm0603, 1%	GENERIC	GENERIC
24	1	R9	1.2Ω	Resistor, sm0603, 10%	GENERIC	GENERIC
25	2	R11, R14	0Ω	Resistor, sm0603, 10%	GENERIC	GENERIC
26	1	R17	1Ω	Resistor, sm0603, 1%	GENERIC	GENERIC
27	2	R18, R19	51kΩ	Resistor, sm0603, 10%	GENERIC	GENERIC
28	1	U1		PWM CONTROLLER, 20Ld QSOP	ISL6420BIAZ	INTERSIL
OPTIONAL COMPONENTS						
29		D2, R6, C20, C28, C23, C25, C30, C33	DO NOT POPULATE			
EVALUATION HARDWARE						
30	4	J4, J5, J6, J7		HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS	KPA8CTP	BERG/FCI
31	4	J1, J 2, J3, J8		1x3 Header	GENERIC	GENERIC
32	4	J1, J2, J3, J8		Connector Jumper	SPC02SYAN	Sullins
33	7	P3, P4, P5, P6		Test Points	1514-2	Keystone

ISL6420BEVAL7Z PCB Layout

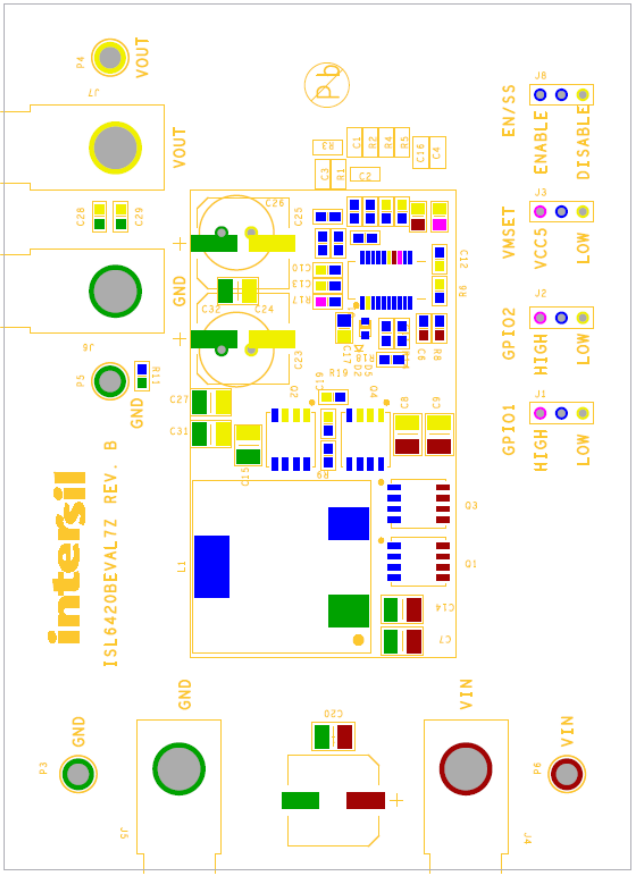

FIGURE 12. TOP SILKSCREEN

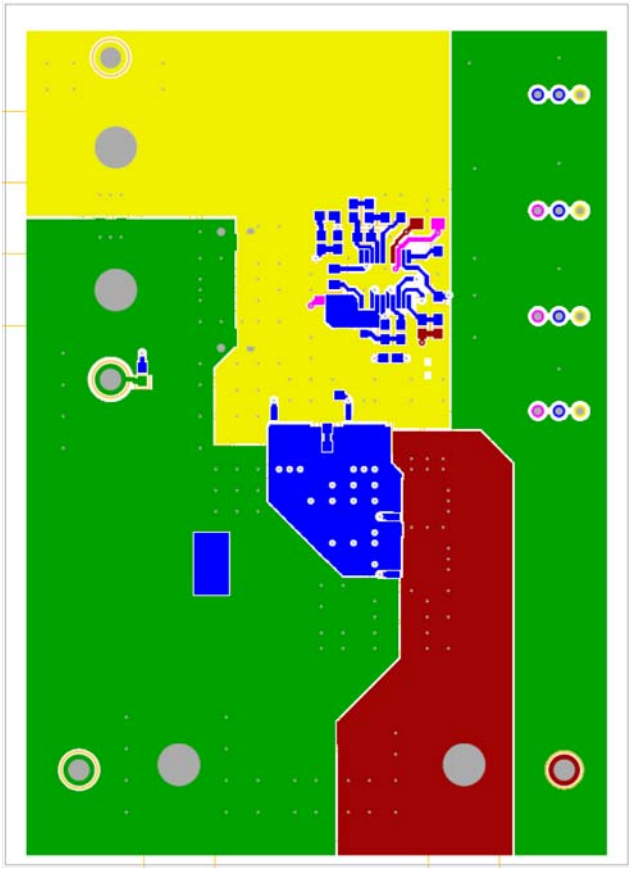

FIGURE 13. TOP LAYER

ISL6420BEVAL7Z PCB Layout (Continued)

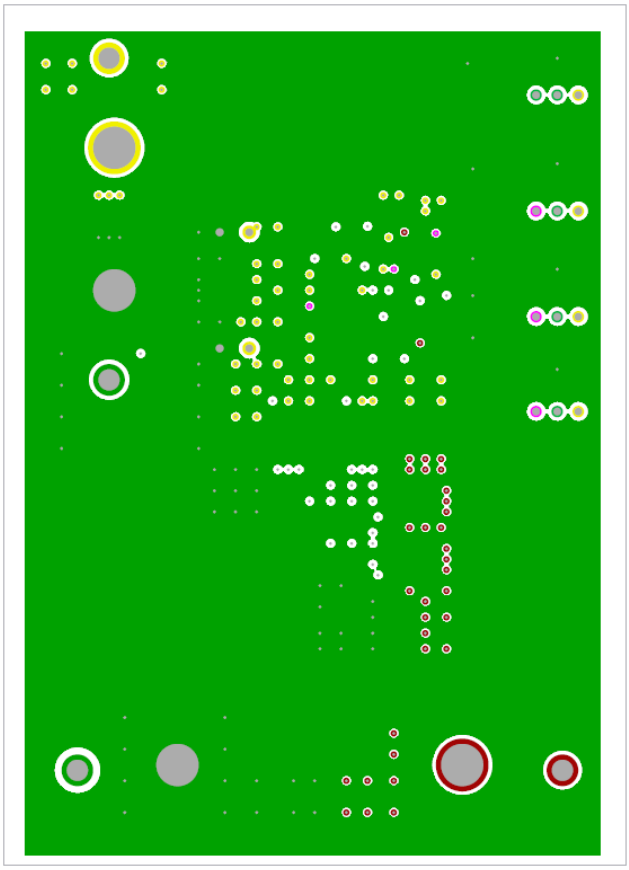

FIGURE 14. SECOND LAYER (SOLID GROUND)

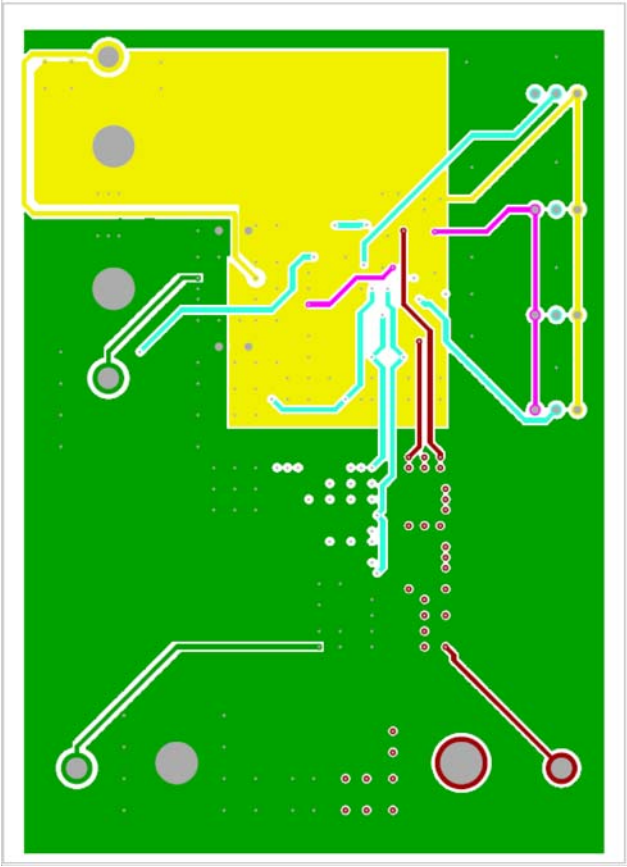

FIGURE 15. THIRD LAYER

ISL6420BEVAL7Z PCB Layout (Continued)

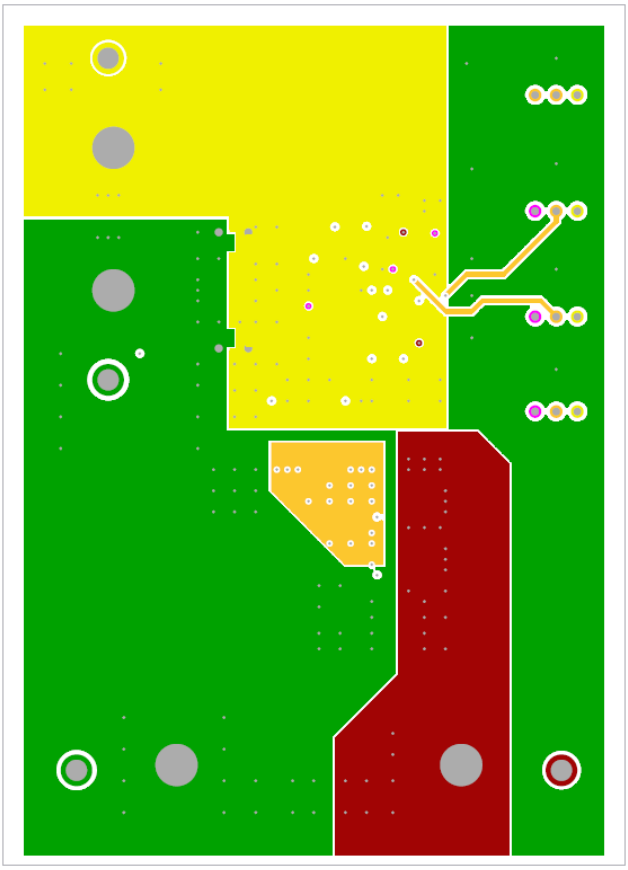

FIGURE 16. BOTTOM LAYER

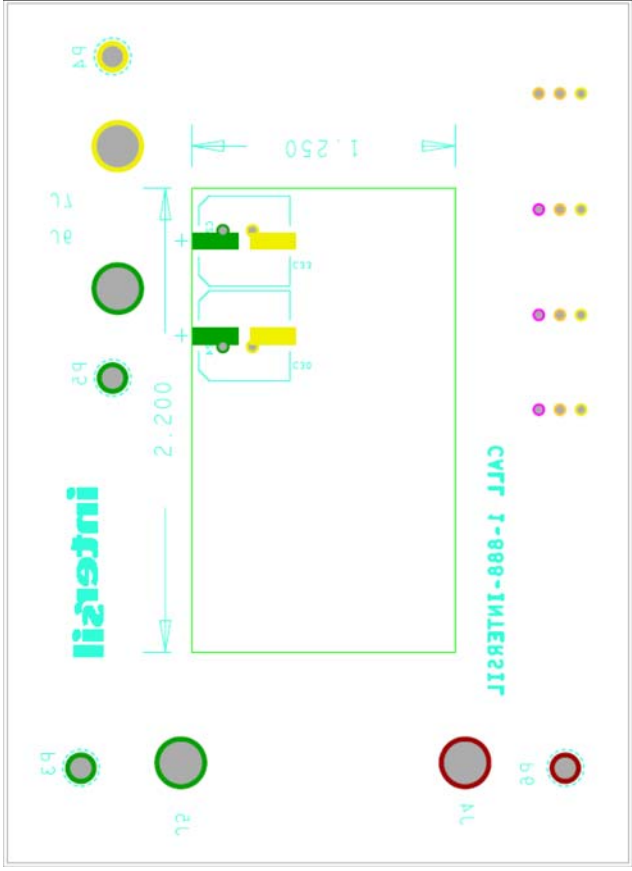

FIGURE 17. BOTTOM SILKSCREEN