

Using the ISL6269 and ISL6269A for 5V VOUT Applications

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Description

This document specifies the requirements for the extended output voltage regulation range of the ISL6269 and ISL6269A Single-Phase Synchronous-Buck PWM controllers. The application space specified within the ISL6269 and ISL6269A datasheets is +7.0V to +25.0V input voltage and +0.6V to +3.3V output voltage. The application space may be amended to accommodate an output voltage of 5V when the requirements of this document are followed.

Requirements

- The input voltage of the converter must be between +12.0V to +25.0V.
- The FCCM pin must be connected to the VCC pin, forcing the converter into continuous conduction mode. If allowed into discontinuous conduction mode at low load, the bootstrap capacitor voltage could discharge to 0V during the time interval between PWM pulses.
- A 499Ω resistor R_{MS} is placed in series with the VO pin to protect the internal ESD diode that is connected to V_{CC} . The ESD diode will conduct current into the V_{CC} node in the unlikely event where the tolerance stack up of V_{CC} , V_{FB} , I_{FB} , V_{OVR} , R_{TOP} , and R_{BOTTOM} results in a voltage sufficient to forward bias the device. Refer to Figure 5.

V_{COMP} and Duty Cycle

A window voltage V_W is referenced with respect to the error amplifier output voltage V_{COMP} , creating an envelope into which the ripple voltage V_R across ripple capacitor C_R is compared. Figure 1 shows PWM pulses being generated as V_R traverses the V_W and V_{COMP} thresholds.

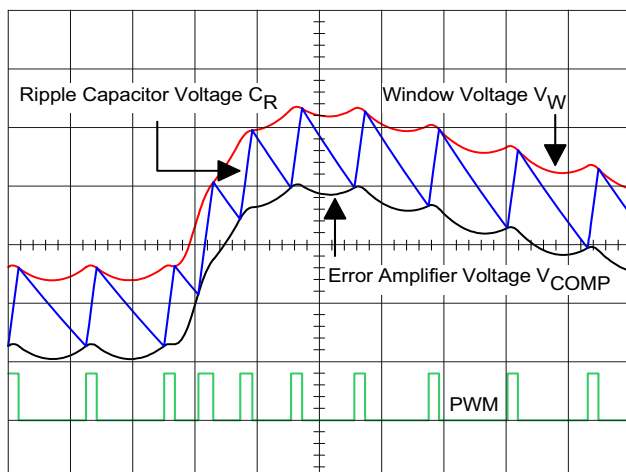


FIGURE 1. MODULATOR LOAD TRANSIENT WAVEFORMS

The static V_{COMP} voltage increases as V_{OUT} , I_{LOAD} , and duty cycle increases. The duty cycle increases as V_{IN} decreases or in response to a load transient. As the slow rate of the transient becomes faster, the ΔV_{COMP} becomes larger. A minimum V_{IN} of 12V has been established so that V_{COMP} does not hit an internal 3.20V clamp in applications where V_{OUT} is programmed to 5V. The voltage clamp ensures that there will be sufficient head room above V_{COMP} so that the window voltage V_W , which can be as large as 900mV, does not saturate at the minimum specified V_{CC} input bias voltage of 4.75V. A graphical representation of the V_{COMP} range is found in Figure 4. The waveforms in Figure 2 show the transient response of the 5V converter at 7V V_{IN} and a transient load of 1Ω. Notice that the duty cycle goes to 100%, V_{OUT} starts falling, and V_{COMP} hits the 3.20V clamp.

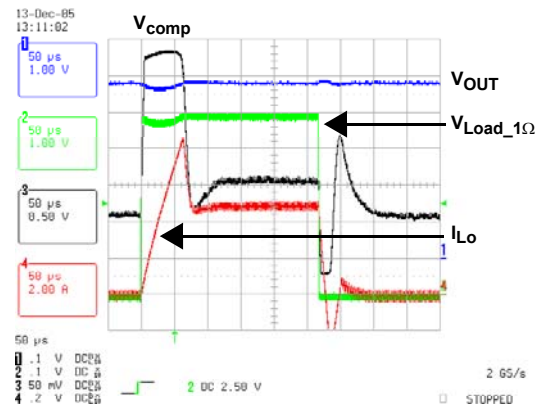


FIGURE 2. TRANSIENT RESPONSE AT 7V V_{IN}

The waveforms in Figure 3 show the transient response of the 5V converter at 15V V_{IN} and a transient load of 1Ω. Notice that V_{OUT} stays well regulated and V_{COMP} avoids the 3.20V clamp.

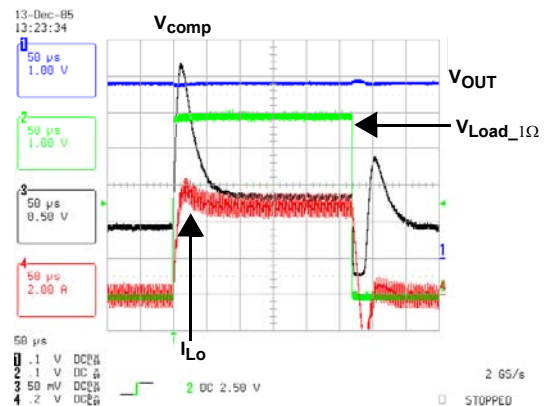


FIGURE 3. TRANSIENT RESPONSE AT 15V V_{IN}

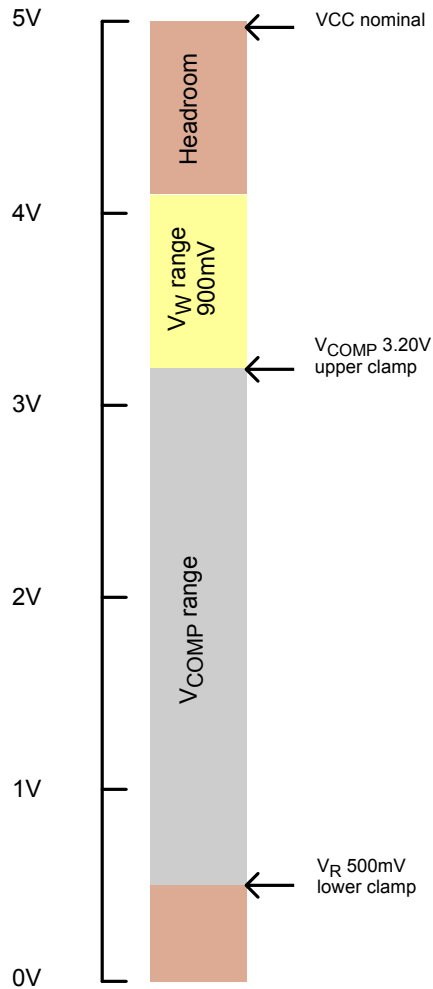


FIGURE 4. V_{COMP} RANGE

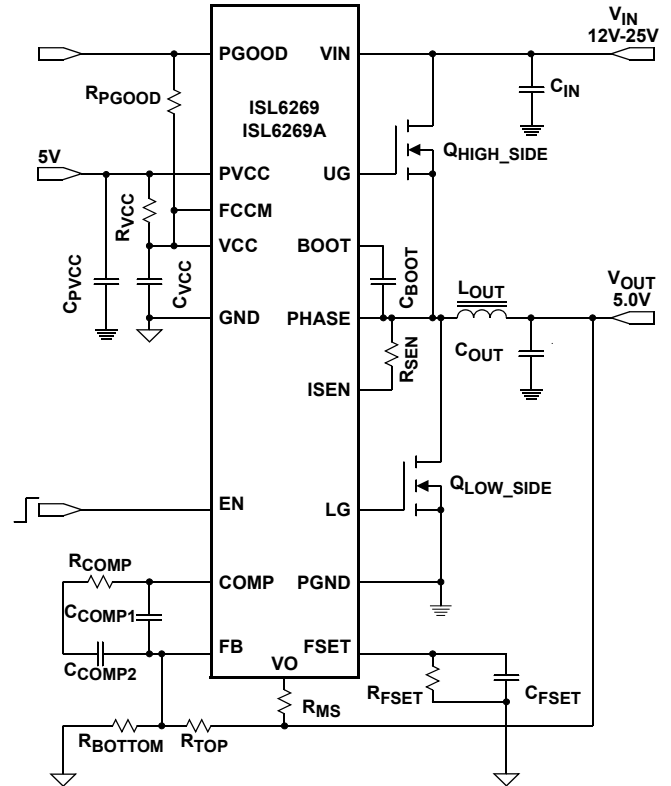


FIGURE 5. SCHEMATIC OF 5V V_{OUT} APPLICATION

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338