ISL70003SEH

Single Event Effects Testing

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Introduction

The intense heavy ion environment encountered in space applications can cause a variety of destructive and non destructive effects in analog circuits, including single event latch-up (SEL), single event gate rupture (SEGR), single event burnout (SEB), single event transients (SET) and single event functional interrupt (SEFI). These effects can lead to system-level failures including disruption and/or permanent damage. For predictable and reliable system operation, these components have to be formally designed and fabricated for SEE hardness, followed by detailed SEE testing to validate the design. This report discusses the results of SEE testing of Intersil's ISL70003SEH, a wide input voltage range (3V to 13.2V) 6A synchronous buck regulator.

Related Documents

- ISL70003SEH Datasheet
- ISL70003SEH Radiation Report
- AN1897 Radiation Hardened and SEE Hardened 3V to 12V, 6A Synchronous Buck Regulator Evaluation Board User's Guide
- AN1915 ISL70003SEH iSim:PE Mode
- AN1924 Total Dose Testing of the ISL70003SEH Radiation Hardened Point Of Load Regulator

Product Description

The ISL70003SEH is a radiation and SEE hardened synchronous buck regulator capable of operating over an input voltage range of 3V to 13.2V. The part is hardened for the total dose and single event effects environments through hardened by design methods and uses a commercial submicron BiCMOS power management process.

With integrated MOSFETs and external loop compensation, this highly efficient single chip power solution provides a tightly regulated output voltage that is externally adjustable from 0.6V to ~85% of the input voltage. Continuous output load current capability is 6A for $T_J \leq +125°C$ and 3A for $T_J \leq +150°C$.

The ISL70003SEH uses voltage mode architecture with feed-forward and switches at a fixed frequency of 500kHz or 300kHz. Loop compensation is externally adjustable to allow for an optimum balance between stability and output dynamic performance. The internal synchronous power MOSFETs are optimized for high efficiency and excellent thermal performance.

The chip features two logic-level disable inputs that can be used to inhibit pulses on the phase (LXx) pins in order to maximize efficiency based on the load current. The ISL70003SEH also supports DDR power applications. It can sink 4A of continuous load current and contains a buffer amplifier for the generating the V_{REF} voltage. High integration, best in class radiation performance and a feature filled design make the ISL70003SEH an ideal choice for a POL solution for space applications.

SEE Summary

A few of the key SEE results are summarized as follows:

- No destructive SEE at LET = 86.4MeV•cm^2/mg
  - Max V_{IN} = 14.7V with 7A load
  - Max V_{IN} = 13.7V with negative inductor valley current
- No SEFIs at LET = 86.4MeV•cm^2/mg with V_{IN} > 5.5V
- No SETs >3% of V_{OUT}, for 13.2V V_{IN} to 3.3V V_{OUT} at 3A load

SEE Test Objective

The ISL70003SEH was tested to determine its susceptibility to destructive effects including single event latch-up (SEL), single event burnout (SEB) and single event gate rupture (SEGR) and to nondestructive effects including single event transient (SET) and single event functional interrupt (SEFI). We will discuss the results in that order. The sample sizes reflected the requirements of MIL-PRF-38535 (QML) and used final version of production parts.

SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 superconducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux and fluence levels needed for advanced radiation testing.

SEE Test Procedure

The part was tested for SEL/SEB/SEGR, using Au ions at zero degree incidence (LET = 86.4MeV•cm^2/mg) with a case temperature of +125°C and single event transient characterized using Au ions with a case temperature of +25°C with the samples at zero degree incident beam angle. Single event functional interrupt testing was done using Au ions and Pr ions with a case temperature of +25°C. SEFI tests conducted with Au ions were done with the samples at zero degree incident beam angle and tests with Pr ions were done with a 15° incident beam angle to achieve an LET of 60MeV•cm^2/mg.

The device under test (DUT) was mounted in the beam line and irradiated with heavy ions of the appropriate species. The parts were assembled in 64 Ld quad flatpack packages with the metal lid removed for beam exposure. The beam was directed onto the exposed die and the beam flux, beam fluence and errors in the device outputs were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable power supplies connected via cable to the DUT. The supply currents were monitored along with the device outputs. All currents were measured with digital ammeters, while all the output waveforms were monitored on a digital oscilloscope for ease of identifying the different types of SEE displayed by the part. Events were captured by triggering on changes in the output1.

SEE Test Set-Up Diagrams

A schematic of the SEE engineering board used during testing is shown in Figure 1.

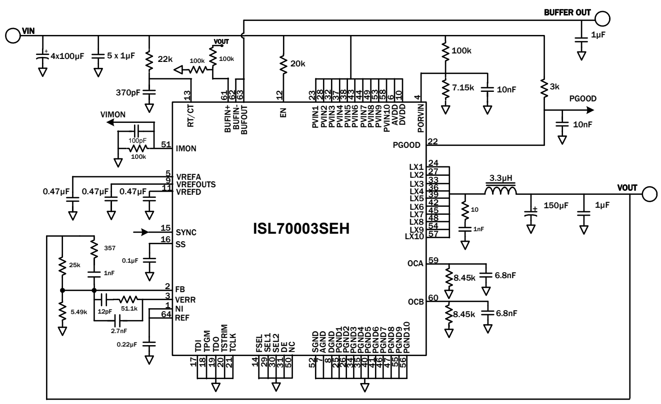


FIGURE 1. ISL70003SEH SEE TEST BOARD SCHEMATIC

Cross-section Calculation

Cross sections (CS) are calculated as shown by Equation 1:

$$CS(LET) = N/F \quad \text{(EQ. 1)}$$

Where:

- CS is the SET cross section (cm^2), expressed as a function of the heavy ion LET
- LET is the linear energy transfer in MeV • cm^2/mg, corrected according to the incident angle, if any.
- N is the total number of SET events
- F is fluence in particles/cm^2

A value of 1/F is the assumed cross section when no event is observed.

Destructive SEE Results

The first testing sequence looked at destructive effects due to burnout, latch-up or gate rupture. A burnout condition is indicated by a permanent change in the device supply current (in any condition) after application of the beam. A permanent change in the supply current of the device may also be indicative of single event gate rupture, as the damaged gate insulator can no longer control the current through integrated MOSFETs. If the increased current can be reset by cycling power, it is termed a non-destructive latch-up.

Destructive SEE test were done with the input voltage set to 13.7V or 14.7V, depending on whether the DUT is sourcing current or sinking current. The samples were irradiated in three configurations: disabled (zero output current but power applied), output current set at +7.0A (sourcing) and output current set at -4.0A (sinking). In all three cases the output voltage was set at 3.3V and the case temperature was maintained at +125°C using an external heater. The failure criterion used for defining destructive SEE was a 5% increase in operating current or a 5% shift in the DC overcurrent protection (OCP) trip point. Failed devices were not further irradiated.

Subsequently, four additional samples, (identified as 1A, 2A, 3A, 4A) were irradiated at 14.7V with an output current of 7A. These samples were then irradiated with the output current set at -4.0A (sinking) at 13.7V. Again these samples were irradiated with the output current set at 0A (open) at 14.7V with 1 of the 4 samples having a significant change in shut down current at this point.

Tables 1 through 4, summarize the results of the destructive SEE testing. The results demonstrate that the device passes the objective maximum in-beam supply voltage specification of 14.7V at the specified LET of 86MeV•cm^2/mg for the disabled and sourcing current with no negative valley inductor current, and of 13.7V in sourcing with negative valley inductor current or in sinking configurations.

Output Voltage SET Results

Test Setup

Single event transient (SET) testing of the ISL70003SEH was carried out with the samples configured as a single-phase converter operating at 3.0A output current. The samples were irradiated using Au ions at a zero degree incident beam angle for an effective LET of 86MeV•cm^2/mg. Two different I/O conditions were tested. The first configuration was a 3V input to 1.8V output and the second was a 13.2V input to 3.3V output. The samples were tested at two different switching frequencies. The first switching frequency was 300kHz generated by the internal oscillator of the ISL70003SEH. The second frequency was 500kHz and was generated by an arbitrary waveform generator whose output was to connect to the SYNC pin of the DUT. The flux for each run was 5.0 x 10^4 ions/cm^2•s. An SET was defined as an output voltage perturbation of ±40mV, with an objective of not exceeding ±3% of the output voltage. The output LC filter of the buck regulator during testing for a 3V input was a 3.3µH inductor with a single 150µF tantalum capacitor in parallel with a 1µF ceramic capacitor for high frequency filtering of the output voltage (see Figure 1). In the high voltage SET testing the inductor was changed to 6.8µH.

Oscilloscope Setup

An oscilloscope was used to capture the deviations of the output. The connections for the scope are described as follows:

Oscilloscope Channel Connections and Settings:

- CH1 = V_{OUT} 50mV/div, trigger on ±40mV window
- CH2 = LX 680mV/div for 3V, 5V/div for 13.2V
- CH3 = V_{ERR} 50mV/div
- CH4 = V_{REF} 50mV/div
- Time scale = 20µs/div

Cross Section Results

Table 5 details the cross section results of the SET testing of the ISL70003SEH. The table is divided into two sections. The top section shows the cross section results with the input to the DUT at 3V. The bottom section shows the results for a 13.2V input to the DUT. Each section compares the results of the cross section due to the use of the internal oscillator versus an external synchronization signal. A total of 8 devices were used for SET testing. Four devices were allocated for the 3V input test and 4 devices for the 13.2V input test. Each device had two runs, each consisting of using the internal versus external oscillator.

TABLE 1. ISL70003SEH DETAILS OF SEB/L TESTS FOR V_{IN} = 14.7V AND DUT DISABLED

TEMP (°C)	V_{IN} (V)	I_{OUT} (A)	LET (MeV•cm²/mg)	SUPPLY CURRENT PRE-EXPOSURE (mA)	SUPPLY CURRENT POST-EXPOSURE (mA)	DESTRUCTIVE EVENTS	CUMULATIVE FLUENCE (PARTICLES/cm²)	CUMULATIVE CROSS SECTION (cm²)	DEVICE ID	SEB
125	14.7	N/A	86.4	97.1	97.3	0	5.0×10^6	2.0×10^{-7}	1	PASS
125	14.7	N/A	86.4	98.5	98.2	0	5.0×10^6	2.0×10^{-7}	2	PASS
125	14.7	N/A	86.4	96.8	97.1	0	5.0×10^6	2.0×10^{-7}	3	PASS
125	14.7	N/A	86.4	99.3	99.1	0	5.0×10^6	2.0×10^{-7}	4	PASS
					TOTAL EVENTS	0				
						OVERALL FLUENCE	2.0×10^7			
							OVERALL CS	5.0×10^{-8}		
								TOTAL UNITS	4	

TABLE 2. ISL70003SEH DETAILS OF SEB/L TESTS FOR V_{IN} = 14.7V SOURCING 7A

TEMP (°C)	V_{IN} (V)	I_{OUT} (A)	LET (MeV•cm²/mg)	SUPPLY CURRENT PRE-EXPOSURE (mA)	SUPPLY CURRENT POST-EXPOSURE (mA)	DESTRUCTIVE EVENTS	CUMULATIVE FLUENCE (PARTICLES/cm²)	CUMULATIVE CROSS SECTION (cm²)	DEVICE ID	SEB
125	14.7	N/A	86.4	97.1	97.1	0	5.0×10^6	2.0×10^{-7}	1	PASS
125	14.7	N/A	86.4	98.6	98.5	0	5.0×10^6	2.0×10^{-7}	2	PASS
125	14.7	N/A	86.4	97.1	97.7	0	5.0×10^6	2.0×10^{-7}	3	PASS
125	14.7	N/A	86.4	99.1	99.1	0	5.0×10^6	2.0×10^{-7}	4	PASS
125	14.7	N/A	86.4	93.6	93.5	0	5.0×10^6	2.0×10^{-7}	1A	PASS
125	14.7	N/A	86.4	94.2	94.6	0	5.0×10^6	2.0×10^{-7}	2A	PASS
125	14.7	N/A	86.4	91.2	92.2	0	5.0×10^6	2.0×10^{-7}	3A	PASS
125	14.7	N/A	86.4	94.1	93.9	0	5.0×10^6	2.0×10^{-7}	4A	PASS
					TOTAL EVENTS	0				
						OVERALL FLUENCE	4.0×10^7			
							OVERALL CS	2.5×10^{-8}		
								TOTAL UNITS	8	

TABLE 3. ISL70003SEH DETAILS OF SEB/L TESTS FOR V_{IN} = 13.7V SINKING 4A

TEMP (°C)	V_{IN} (V)	I_{OUT} (A)	LET (MeV•cm^2/mg)	SUPPLY CURRENT PRE-EXPOSURE (mA)	SUPPLY CURRENT POST-EXPOSURE (mA)	DESTRUCTIVE EVENTS	CUMULATIVE FLUENCE (PARTICLES/cm^2)	CUMULATIVE CROSS SECTION (cm^2)	DEVICE ID	SEB
125	13.7	N/A	86.4	93.9	93.9	0	5.0×10^6	2.0×10^{-7}	5	PASS
125	13.7	N/A	86.4	94.8	94.3	0	5.0×10^6	2.0×10^{-7}	6	PASS
125	13.7	N/A	86.4	94.4	94.5	0	5.0×10^6	2.0×10^{-7}	7	PASS
125	13.7	N/A	86.4	94.9	95.2	0	5.0×10^6	2.0×10^{-7}	8	PASS
125	13.7	N/A	86.4	91.1	90.8	0	1.0×10^7	1.0×10^{-7}	1A	PASS
125	13.7	N/A	86.4	91.9	92.5	0	1.0×10^7	1.0×10^{-7}	2A	PASS
125	13.7	N/A	86.4	89.2	89.8	0	1.0×10^7	1.0×10^{-7}	3A	PASS
125	13.7	N/A	86.4	91.8	91.8	0	1.0×10^7	1.0×10^{-7}	4A	PASS
					TOTAL EVENTS	0				
						OVERALL FLUENCE	6.0×10^7			
							OVERALL CS	1.7×10^{-8}		
								TOTAL UNITS	8	

TABLE 4. ISL70003SEH DETAILS OF SEB/L TESTS FOR V_{IN} = 14.7V, OUTPUT OPEN

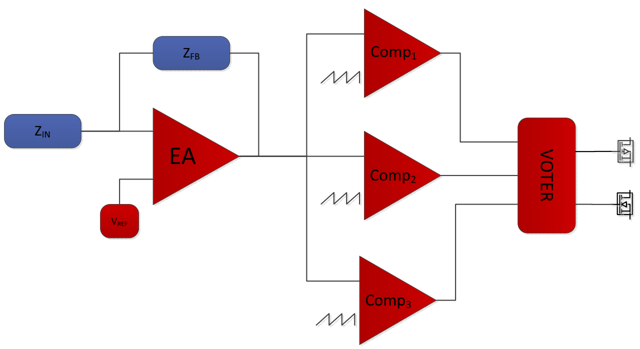
TEMP (°C)	V_{IN} (V)	I_{OUT} (A)	LET (MeV•cm^2/mg)	SUPPLY CURRENT PRE-EXPOSURE (mA)	SUPPLY CURRENT POST-EXPOSURE (mA)	DESTRUCTIVE EVENTS	CUMULATIVE FLUENCE (PARTICLES/cm^2)	CUMULATIVE CROSS SECTION (cm^2)	DEVICE ID	SEB
125	14.7	N/A	86.4	92.2	92.3	0	1.5×10^7	6.7×10^{-8}	1A	PASS
125	14.7	N/A	86.4	94.6	94.6	0	1.5×10^7	6.7×10^{-8}	2A	PASS
125	14.7	N/A	86.4	92.1	91.6	0	1.5×10^7	6.7×10^{-8}	3A	PASS
125	14.7	N/A	86.4	94.2	95.5	1	1.5×10^7	6.7×10^{-8}	4A	FAIL
					TOTAL EVENTS	1 (Shutdown Current increased from 6.9mA to >22mA)				
						OVERALL FLUENCE	6.0×10^7			
							OVERALL CS	1.7×10^{-8}		
								TOTAL UNITS	4	

TABLE 5. ISL70003SEH DETAILS OF THE SET CROSS SECTION

V_{IN} (V)	V_{OUT} (V)	NUMBER OF DEVICES	FSW (kHz)	EFFECTIVE LET (MeV·cm^2/mg)	FLUENCE PER RUN (PARTICLES/cm^2)	NUMBER OF RUNS	TOTAL SET EVENTS	EVENT CS (cm^2)
3.0	1.8	4	300 (internal)	86	1.0×10^7	4	1534	3.84×10^{-5}
3.0	1.8	4	500 (external)	86	1.0×10^7	4	1359	3.40×10^{-5}
				Total Fluence per run	2.0×10^7			
					Total Runs	8		
						Total SET Events	2893	
							Total Cross Section	7.23×10^{-5}
13.2	3.3	4	300 (internal)	86	1.0×10^7	4	1216	3.04×10^{-5}
13.2	3.3	4	500 (external)	86	1.0×10^7	4	1889	4.72×10^{-5}
				Total Fluence per run	2.0×10^7			
					Total Runs	8		
					Total SET Events		3105	
							Total Cross Section	7.76×10^{-5}

Voltage Deviation Results

Compared to other Intersil point of load (POL) regulators, the ISL70003SEH employs a quasi-triple redundant control loop to give system designers the ability to achieve an optimal balance between stability and dynamic response. The quasi redundant loop employs only one error amplifier in the control loop of the regulator. This was needed for external compensation of the error amplifier. There is still however redundancy in the PWM circuitry, as the output of the error amplifier is connected to three comparators and then its output goes through a voter circuitry to drive the internal MOSFETs, (see Figure 2).



* Blue fill indicates external compensation

FIGURE 2. ISL70003SEH QUASI REDUNDANT CONTROL LOOP

Due to the lack of three independent error amplifiers, the ISL70003SEH is expected to have larger voltage deviations due to SETs than its predecessors. However, it is still expected that the LX pulse train would only have a single pulse perturbation due to an SET since the voter logic is still employed in the PWM circuitry.

HISTROGRAM PLOTS

Figures 3 through 10 show histograms of the magnitude of the voltage deviation for each run of SET testing for 13.2V input test. They plot both the negative and positive transients counts and are binned in 10mV increments up to 100mV, which represents 3% of the nominal 3.3V output voltage.

A count that falls into the bin represents an SET whose deviation is equal to or larger than the previous bin but less than that bin. For example, in Figure 3 there are approximately 300 positive SET counts that are classified in the 40mV bin. This means that there were ~300 positive SETs that were equal to or larger than 30mV but less than 40mV.

For the 13.2V input to 3.3V output configuration the SET data shows that majority of the SETs were positive and between 30mV and 40mV, which translates to 0.9% to 1.2% of the output voltage. The max deviation was a negative transient with 80mV in magnitude found in run 217 with a count of 2. Total deviation of 80mV translates to 2.4% of the output voltage.

Figures 11 through 18 show the histogram of the magnitude of the voltage deviation for the 3V input to 1.8V output configuration. The binning is done the same way as the high voltage tests, except the max bin is now 110mV. The SET data shows the majority of the SETs were in the negative direction and between 50mV to 60mV, which is 2.7% to 3.3% of the output voltage. There were three captures that fell under the 110mV bin, one in run 201 and two in run 202. The maximum deviation was 105mV in run 201 and the ones in run 202 were 100.2mV and 100.4mV deviations. The maximum deviation of 105mV is 5.8% of the output voltage. To minimize SETs for low input voltages, it is recommended to add more output capacitance, which is typical for a low output voltage that needs to meet tight regulation. All of the SEE testing was done with a single 150µF tantalum capacitor on the output.

Histogram Plots for 13.2V Input

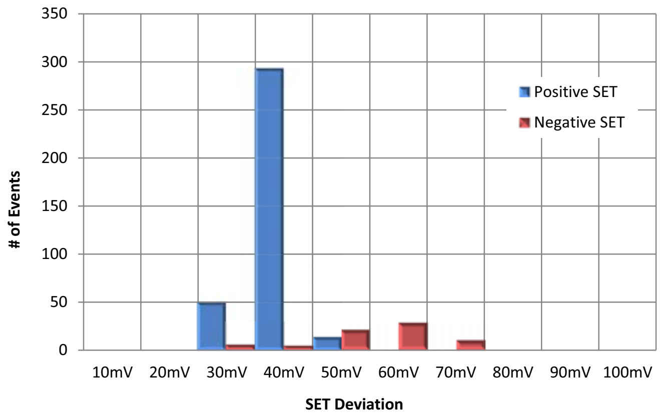


FIGURE 3. HISTOGRAM PLOT FOR RUN 215, f_{SW} = 300kHz INTERNAL OSCILLATOR

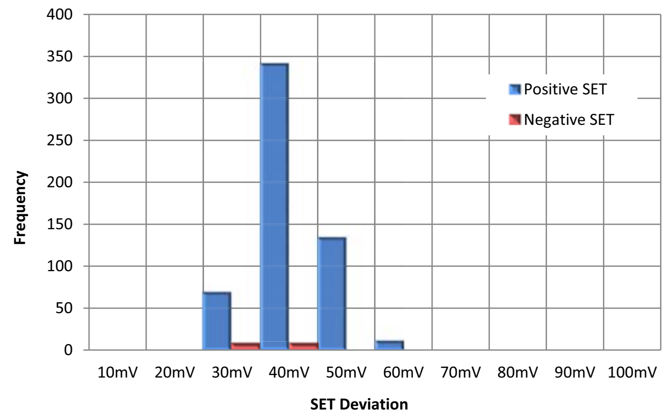


FIGURE 4. HISTOGRAM PLOT FOR RUN 216, f_{SW} = 500kHz EXTERNAL OSCILLATOR

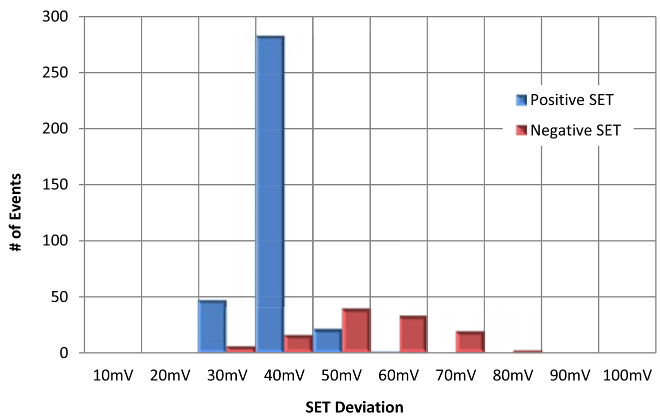


FIGURE 5. HISTOGRAM PLOT FOR RUN 217, f_{SW} = 300kHz INTERNAL OSCILLATOR

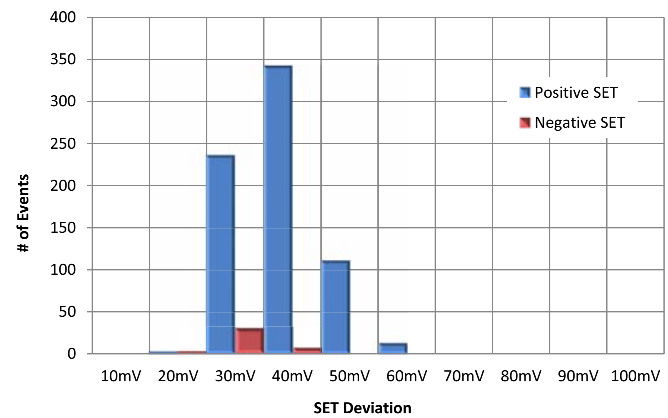


FIGURE 6. HISTOGRAM PLOT FOR RUN 218, f_{SW} = 500kHz EXTERNAL OSCILLATOR

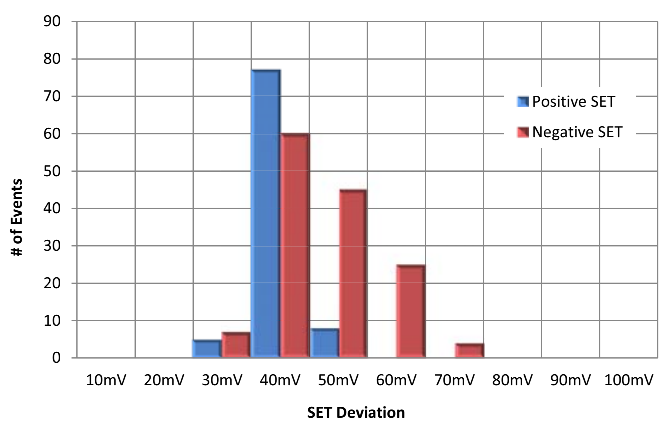


FIGURE 7. HISTOGRAM PLOT FOR RUN 219, f_{SW} = 300kHz INTERNAL OSCILLATOR

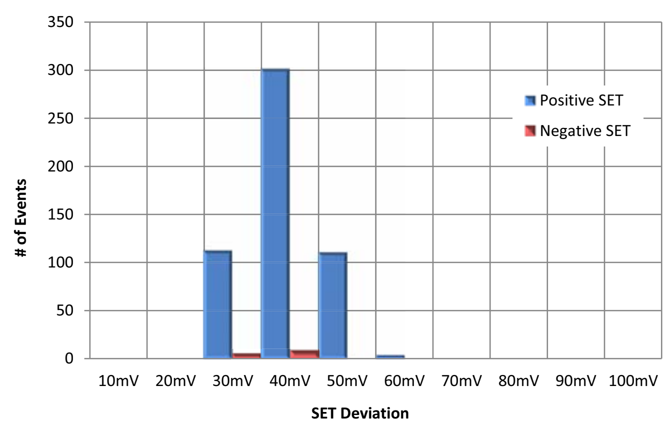


FIGURE 8. HISTOGRAM PLOT FOR RUN 220, f_{SW} = 500kHz EXTERNAL OSCILLATOR

Histogram Plots for 13.2V Input (Continued)

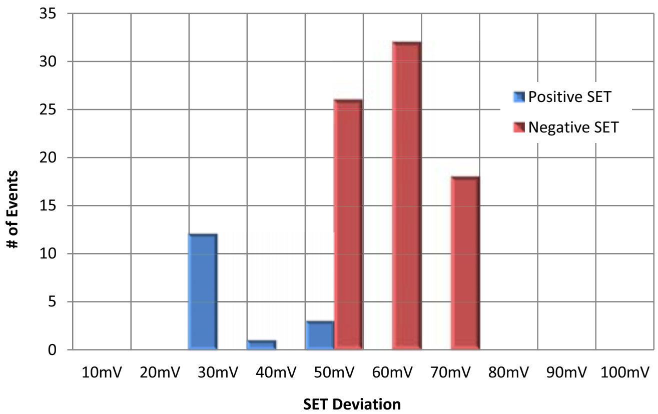


FIGURE 9. HISTOGRAM PLOT FOR RUN 221, f_{SW} = 300kHz INTERNAL OSCILLATOR

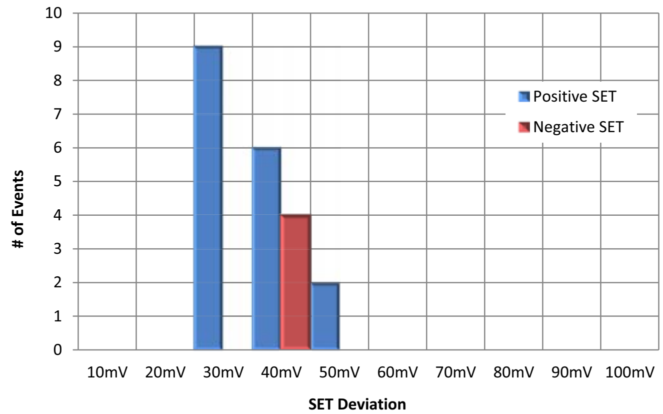


FIGURE 10. HISTOGRAM PLOT FOR RUN 222, f_{SW} = 500kHz EXTERNAL OSCILLATOR

Histogram Plots for 3V Input

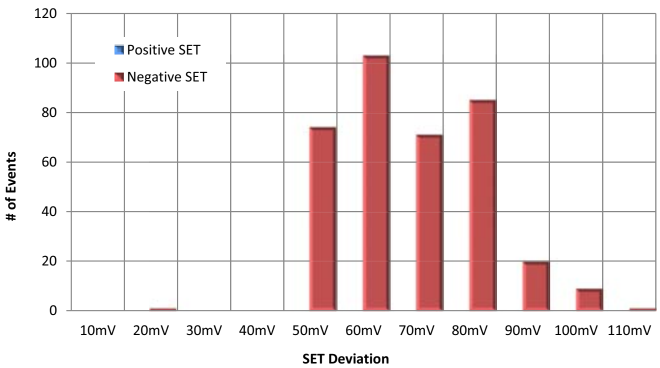


FIGURE 11. HISTOGRAM PLOT FOR RUN 201, f_{SW} = 300kHz INTERNAL OSCILLATOR

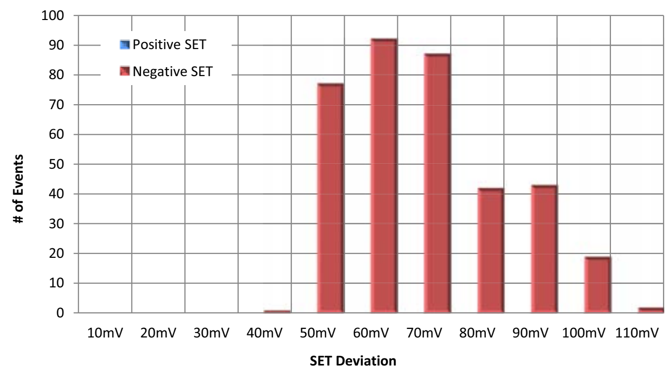


FIGURE 12. HISTOGRAM PLOT FOR RUN 202, f_{SW} = 500kHz EXTERNAL OSCILLATOR

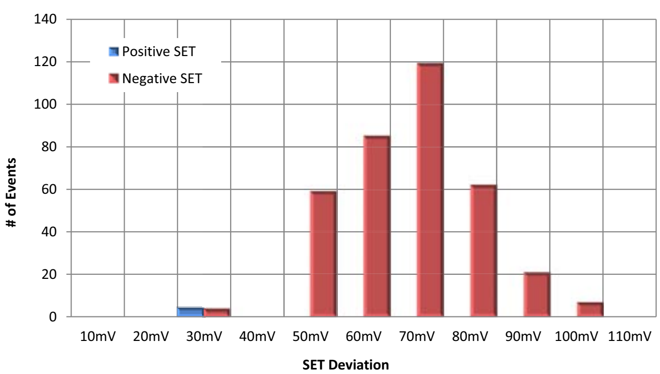


FIGURE 13. HISTOGRAM PLOT FOR RUN 204, f_{SW} = 300kHz INTERNAL OSCILLATOR

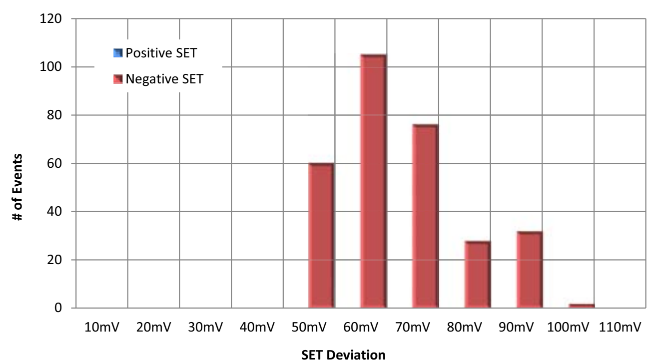


FIGURE 14. HISTOGRAM PLOT FOR RUN 205, f_{SW} = 500kHz EXTERNAL OSCILLATOR

Histogram Plots for 3V Input (Continued)

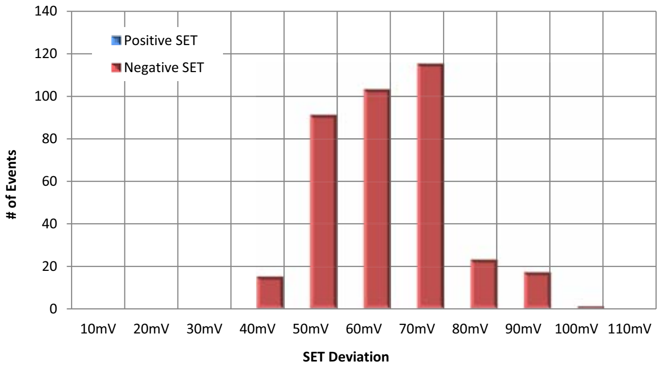


FIGURE 15. HISTOGRAM PLOT FOR RUN 207, f_{SW} = 300kHz INTERNAL OSCILLATOR

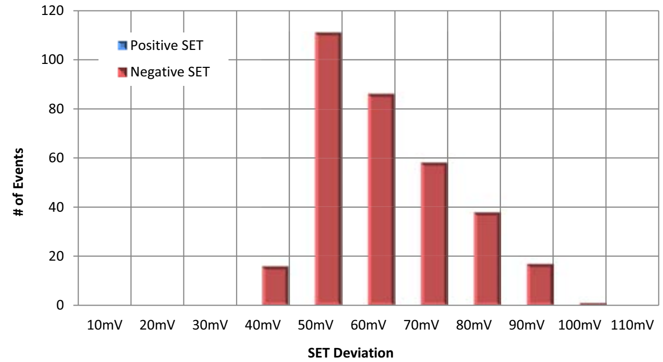


FIGURE 16. HISTOGRAM PLOT FOR RUN 208, f_{SW} = 500kHz EXTERNAL OSCILLATOR

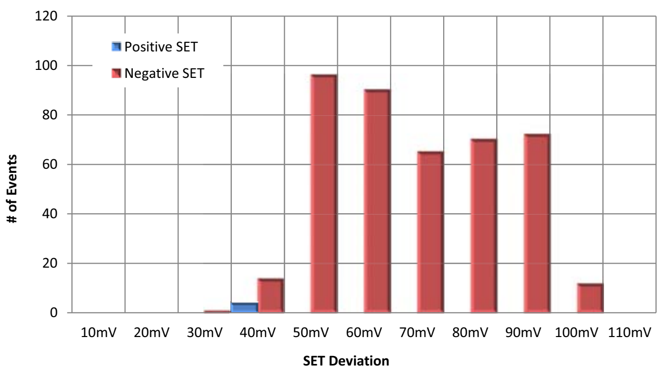


FIGURE 17. HISTOGRAM PLOT FOR RUN 210, f_{SW} = 300kHz INTERNAL OSCILLATOR

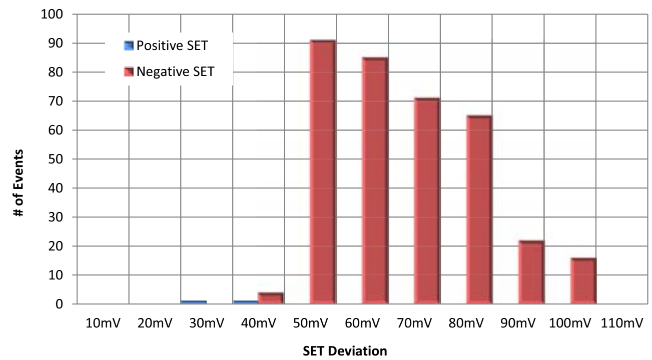


FIGURE 18. HISTOGRAM PLOT FOR RUN 211, f_{SW} = 500kHz EXTERNAL OSCILLATOR

SINGLE EVENT TRANSIENT RESPONSE

The previous section provided data on the peak magnitude of the deviation on the output voltage due to a SET. This section provides example captures of the transient seen during SEE testing. Figures 19 and 20 are positive and negative SET captures for the 3V input to 1.8V output configurations. Figures 21 and 22 show similar SET captures for 13.2V input to 3.3V output operation.

Figure 19 represents a typical negative transient, caused by a shortened pulse in the cycle previous to time = 0, followed by three maximum duty cycle pulses. There is clearly only a one pulse disruption followed by the regulator adjusting its duty cycle to recover from the disruption of normal operation. Recovery is very controlled and duration is ~40µs. The actual time below 3% is even shorter (<20µs). The response of the output is similar to a transient load step in which the capacitance value dominates the droop. As previously mentioned, adding a second capacitor on the output would reduce the deviation by approximately half.

Figure 20 shows a positive transient when the DUT is operated from a 3V input. Two clock cycles before trigger captures at t = 0, one can see the increase in duty cycle of the LX pulse train due to the ion strike, which leads to the positive SET. The larger duty cycle increases the output voltage and the regulator corrects the error by terminating the following LX pulses at lower duty cycles. The recovery of the output voltage is controlled with no oscillations and is quick with recovery to nominal output voltage in less than 20µs.

Figure 21 is an example of a positive SET when the DUT is operated from a 13.2V input. A single elongated pulse is seen in the LX plot, in the clock cycle before time = 0 followed by a shortened pulse due to the regulator trying to recover from the increased output voltage. Recovery is controlled and less than 10µs. Once again the LX pulse train only shows one disturbance due to an SET.

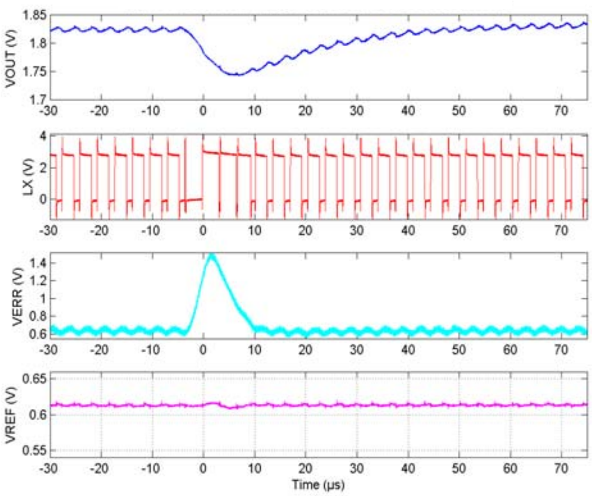


FIGURE 19. NEGATIVE SET, RUN 201 CAPTURE 3, V_{IN} = 3V

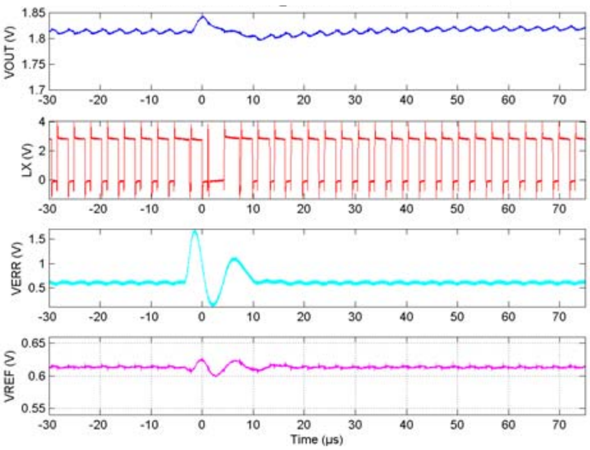


FIGURE 20. POSITIVE SET, RUN 204 CAPTURE 204, V_{IN} = 3V

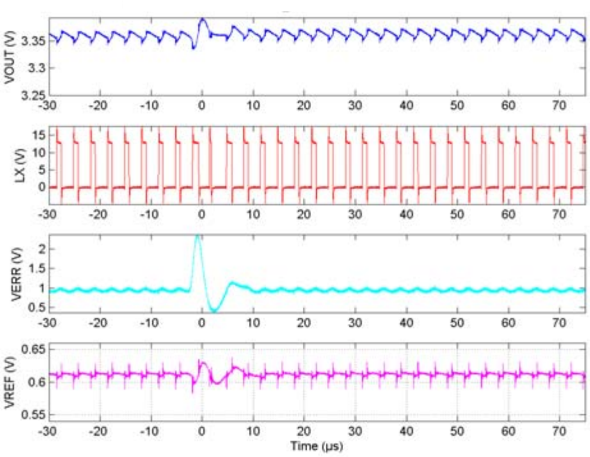


FIGURE 21. POSITIVE SET, RUN 217 CAPTURE 117, V_{IN} = 13.2V

Figure 22, shows a negative transient when the DUT is configured to operate from a 13.2V input. A skipped LX pulse causes a droop in the output voltage. As a result, the error amplifier's output increases and induces the next pulses to have a longer on time to regulate the output voltage to its steady state value. There is only one disturbance in the LX pulse train that is induced by the heavy ion strike.

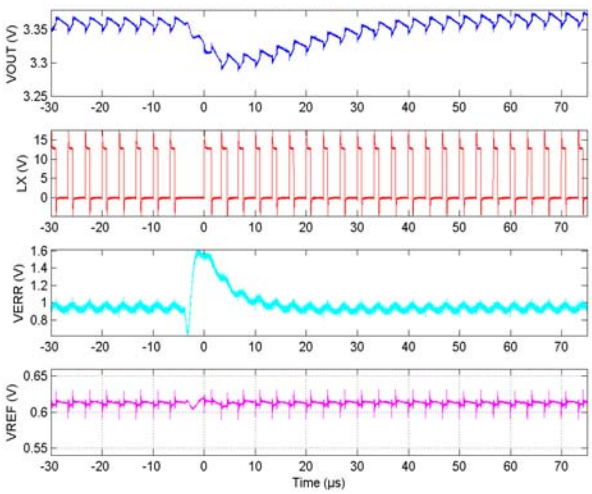


FIGURE 22. NEGATIVE SET, RUN 217 CAPTURE 242, V_{IN} = 13.2V

Single Event Functional Interrupt Results

Single event functional interrupt (SEFI) phenomena were encountered in previous testing of POL regulators, therefore, it was an extensive part of SEE testing [1] [2]. SEFI phenomena for the ISL70001SRH and ISL70002SRH were encountered only at low supply voltage (3V), hence there was an expectation to encounter SEFI at the same supply level. A single event functional interrupt is defined as a non destructive event resulting in the disruption of normal operation of the part, followed by a recovery to normal operation through a soft-start cycle.

For the SEFI tests, the input voltages tested were 3V, 5.5V and 13.2V. The samples were irradiated at an LET of 86 MeV•cm^2/mg and 60 MeV•cm^2/mg, using Au and Pr ions respectively. The PGOOD pin of the DUT was monitored through a scope and counts were taken as the scope triggered on a falling edge of PGOOD. The trigger level was set to 50% of the PGOOD pull-up voltage. Other monitored signals included VOUT, REF and VREFA.

SEFI events were observed at 3V input and LET = 86 MeV•cm^2/mg only. No SEFI's were seen with 5.5V or 13.2V input at LET 86.4 MeV•cm^2/mg and with 3V input at LET 60 MeV•cm^2/mg. Table 6 summarizes the SEFI cross section results of the ISL70003SEH.

TABLE 6. ISL70003SEH SEFI CROSS SECTION SUMMARY

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	LET (MeV•cm^2/mg)	SPECIES	FLUENCE (PARTICLES/cm^2)	RUNS	SEFI EVENTS	CUMULATIVE CROSS SECTION (cm^2)
3.0	1.8	3	86.4	Au	1.0×10^7	8	44	5.5×10^{-7}
3.0	1.8	3	60	Pr	1.0×10^7	4	0	2.5×10^{-8}
5.5	1.8	3	86.4	Au	1.0×10^7	4	0	2.5×10^{-8}
13.2	3.3	3	86.4	Au	1.0×10^7	8	0	1.3×10^{-8}

All SEFI signatures observed showed a spontaneous recovery to normal operation. Some were restarts, while others were a hiccup cycle (which is a dummy soft-start cycle) followed by a restart. The recovery time is a function of the value of the soft-start capacitor used as an SEE fixture. The SEFI cross section for 3V input was 5.5 x $10^{-7}/cm^2$, indicating a very low probability of occurrence of this phenomenon.

Figure 23 shows an ISL70003SEH SEFI signature at LET = 86.4 MeV • cm^2/mg at 3V input. The PGOOD output drops to zero as output voltage decays to zero. VREF remains at 600mV and VREFA remains at 3V indicating an active regulator. The horizontal axis is calibrated at 100µs per division.

Figure 24 shows another SEFI response with the time scale changed to 2ms per division. This response shows the regulator starting up ~1ms after the SEFI occurs. This is consistent with the delay interval of 512 clock cycles seen after fault condition, such as overcurrent protection occurs.

Figure 25 shows a SEFI signature with a hiccup cycle. In this signature the regulator goes through a dummy soft-start before it starts backup. In all cases, the regulator does not need a reset or removal of power to restart.

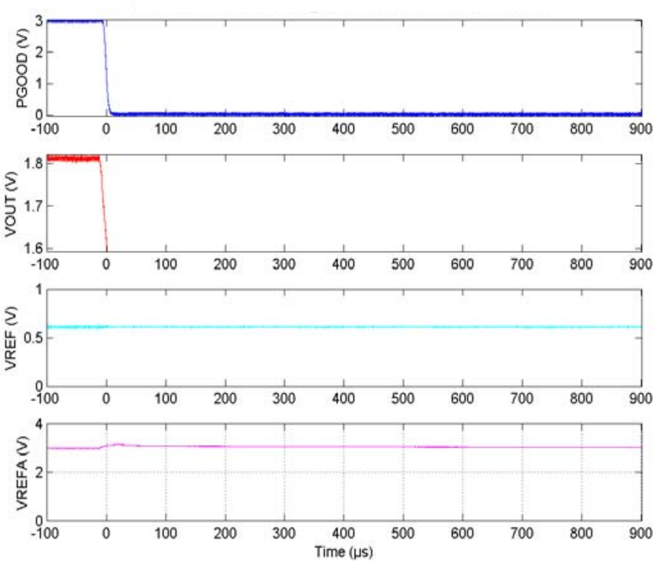


FIGURE 23. SEFI, RUN 204 CAPTURE 2, V_{IN} = 3V

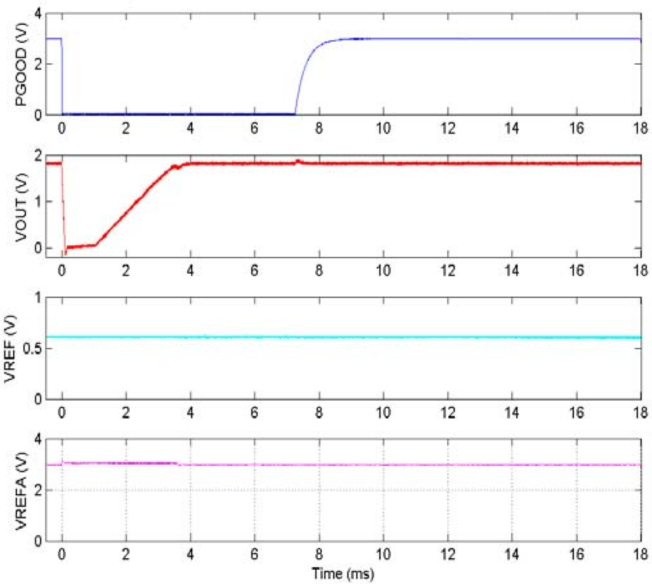


FIGURE 24. SEFI, RUN 208 CAPTURE 1, V_{IN} = 3V

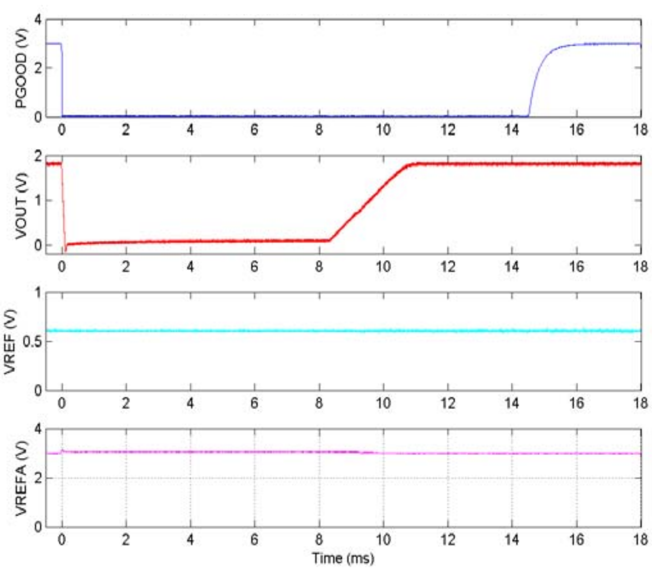


FIGURE 25. SEFI, RUN 204 CAPTURE 1, V_{IN} = 3V

SET Results of Other Outputs

The ISL70003SEH is a highly integrated buck regulator, which features a current monitor output and internal buffer to generate the V_{REF} voltage necessary in DDR power applications. In conjunction with SET and SEFI testing of the output voltage, both of these outputs were also monitored during SET testing. These features were not intended to be single event transient immune therefore, it is important to characterize their SET behavior with cross section results and composite plots of the transient response.

IMON Current Sense Output SET Results

The ISL70003SEH provides a current monitor function through the IMON pin. Current monitoring informs designers if down steam loads are operating as expected and to measure the overall performance of a system. The IMON pin outputs a high speed analog current source that is proportional to the sensed peak current through the ISL70003SEH. In typical applications, a resistor R_{IMON} is connected to the IMON pin to convert the sensed current to voltage, V_{IMON}.

For 13.2V input tests R_{IMON} was set to 100kΩ and for 3V input test R_{IMON} = 50kΩ. In both configurations there was a 100pF ceramic capacitor to reduce the switching noise in the IMON signal. A trigger window of ±80mV was used to capture and count the events on IMON. This equates to a ±2.7% deviation with respect to the 3A load current.

Figure 26 is a composite plot of the first 50 captures of run 215. In this run the input voltage was 13.2V, output conditions were 3.3V output with 3A load and the regulator switching at 300kHz. The transients are both positive and negative with a controlled response to its nominal value within 100µs. Peak transients in this example is ~300mV, which equates to 10% of the load current. Since the IMON output is not intended to be a real time representation of the current through the regulator but a long term diagnostic tool to evaluate the overall performance of the system's load, it is more important that an SET does not cause a permanent shift in the average value than the actual peak deviation induced by the SET.

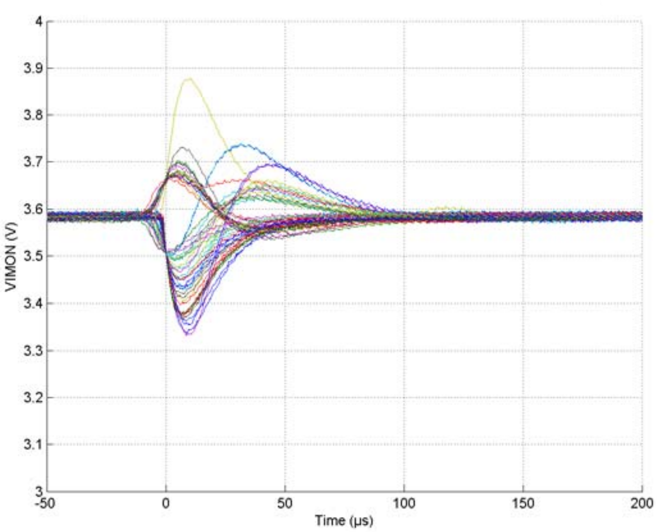


FIGURE 26. IMON COMPOSITE SET PLOT, RUN 215, V_{IN} = 13.2V

Figure 27 is a composite plot of the first 50 captures of run 220. In this run the input voltage was 13.2V, output conditions were 3.3V output with 3A load and the regulator switching at 500kHz. Due to the higher switching frequency, the peak current through the regulator is smaller, this is reflected by the average VIMON being lower in this figure compared to Figure 26. The response is similar to previous composite plot, except for the one railed out transient. In a worst case condition a SET on the IMON circuitry could cause the output signal to rail to in the internal bias (VREFA) of the ISL70003SEH.

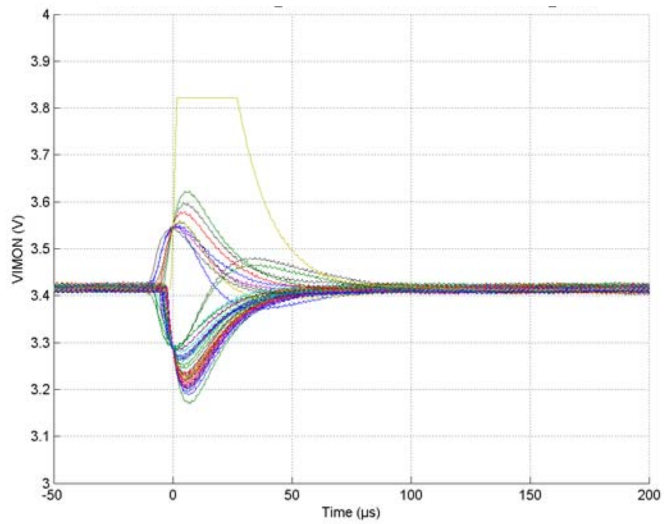


FIGURE 27. IMON COMPOSITE SET PLOT, RUN 220, V_{IN} = 13.2V

Figures 28 and 29 show the results with a 3V input switching at 300kHz and 500kHz, respectively. R_{IMON} = 50kΩ the VIMON average voltage is approximately half of the high input voltage configuration. Figure 29 the IMON signal is railed below the capture window. In a worst case condition, the IMON signal can swing to ground. However, the signal recovers within 100µs to its nominal value indicating there has been no permanent change in the load current

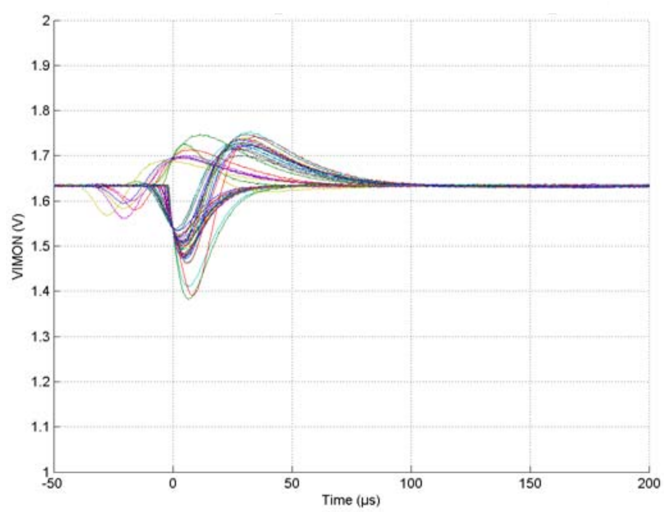


FIGURE 28. IMON COMPOSITE SET PLOT, RUN 207, V_{IN} = 3V

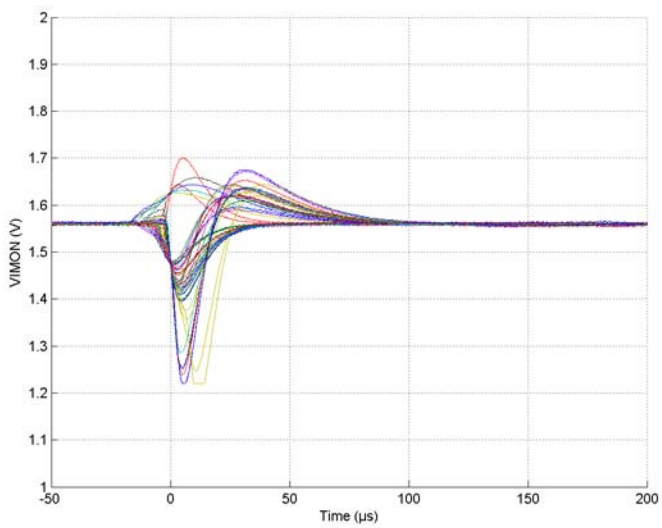


FIGURE 29. IMON COMPOSITE SET PLOT, RUN 211, V_{IN} = 3V

Table 7 gives details of the cross section for the IMON output signal. All tests were done with Au ions at zero degrees for an LET of 86.4MeV•cm2/mg. Four devices were run for each configuration, however for the 3V input test the first runs had erroneous trigger conditions. The captures were terminated early and the data is not used in the calculations.

Buffer Output SET Results

The buffer amplifier is used to generate the reference voltage (V_{REF}) for the DDR memory chips. Sourcing capability of the buffer amplifier is 10mA typical and needs a minimum of 1µF load capacitance for stability. Typical applications will tie the output voltage of the regulator through an R/R resistor divider and configure the amplifier in unity gain. Figure 1 shows the board included two 100k resistors to divide the output voltage by half and connect to the non-inverting input of the buffer amplifier. The amp was configured in unity gain with a 1µF capacitor load. Two devices of each varying input voltage had an additional 62.5Ω load to test the device at no load and loaded condition. In DDR application, the V_{REF} connection is a high impedance input and the buffer amplifier, will have very light load.

Table 8 shows the cross section results of the buffer amplifier. An SET was characterized as a ±40mV deviation of buffer output, which coincides with the limit on V_{REF} for DDRI applications. The table also clearly shows the effect of loading on the counts of the SET. As mentioned before, DDR applications will have very light to no load on the buffer amplifier, which is a plus due to the small cross sections achieved in the no load condition.

TABLE 7. ISL70003SEH IMON SET CROSS SECTION SUMMARY

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	FSW (kHz)	LET (MeV•cm^2/mg)	SPECIES	CUMULATIVE FLUENCE (PARTICLES/cm^2)	EVENTS	CUMULATIVE CROSS SECTION (cm^2)
3.0	1.8	3	300	86.4	Au	3.0×10^7	3490	1.2×10^{-4}
3.0	1.8	3	500	86.4	Au	3.0×10^7	3456	1.2×10^{-4}
13.2	3.3	3	300	86.4	Au	4.0×10^7	5008	1.3×10^{-4}
13.2	3.3	3	500	86.4	Au	4.0×10^7	6137	1.5×10^{-4}

TABLE 8. ISL70003SEH BUFFER AMPLIFIER SET CROSS SECTION SUMMARY

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	BUFFER LOAD (Ω)	LET (MeV•cm^2/mg)	SPECIES	CUMULATIVE FLUENCE (PARTICLES/cm^2)	EVENTS	CUMULATIVE CROSS SECTION (cm^2)
3.0	1.8	3	OPEN	86.4	Au	4.0×10^7	1	2.5×10^{-8}
3.0	1.8	3	62.5	86.4	Au	4.0×10^7	1979	4.95×10^{-5}
13.2	3.3	3	OPEN	86.4	Au	4.0×10^7	4	1.0×10^{-7}
13.2	3.3	3	62.5	86.4	Au	4.0×10^7	3866	9.67×10^{-5}

Figure 30 shows the composite plot for 3V input configuration and the buffer unloaded. The graph only shows one true SET of the buffer amplifier, the other captures are due to the SEFIs phenomenon. The peak deviation is ~35mV and recovery is ~75µs after the peak. The response is controlled dominated by the slew rate of the buffer amplifier and exhibits no oscillations. A typical DDR memory will have in the order of meaning will have somewhere around 20µF to 30µF of capacitive loading on the buffer output, which will help further with SET mitigation.

Figure 31 shows the SET composite plot of the first 50 captures of run 211. The input voltage is 3V and the buffer output is loaded with 62.5Ω. The SET are mainly negative most likely due to the load resistor to ground. Peak deviations are less than 50mV.

Figure 32 is the composite plot of run 215 with an input voltage of 13.2V and the buffer not resistively loaded. Most likely the only SET due to an ion hit on the buffer circuitry is the positive going trace. The other traces are due to SETs on the output voltage propagating through the resistor divider connected to the non- inverting input of the buffer amp. In DDR applications the V_{REF} signal needs to track half of the VDDQ voltage [3]. In our configuration the output voltage of the ISL70003SEH could be thought of as the VDDQ voltage and the buffer amplifier is tracking the voltage as intended.

Figure 33 further emphasizes the theory that in Figure 32 there is only one true SET due to the buffer amp. Figure 33 shows the composite plot of run 217. The device is configured in similar fashion and the responses seen on this plot is very similar to the positive SET in Figure 32. In the calculations for cross section mentioned previously the SET induced by tracking of the output voltage were not used.

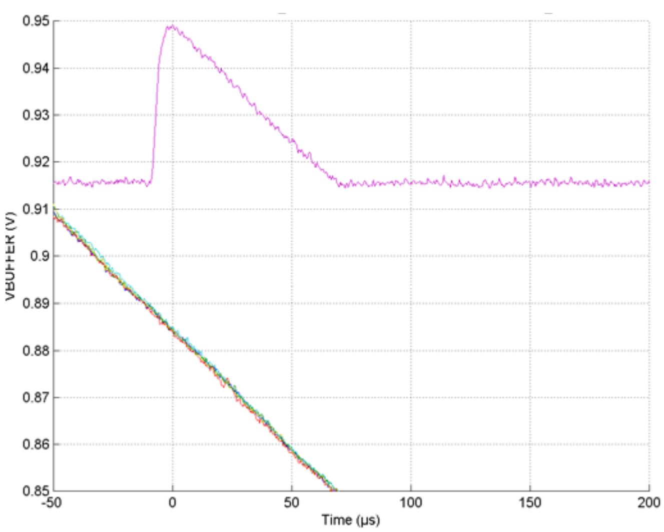


FIGURE 30. BUFFER COMPOSITE SET PLOT, RUN 201, V_{IN} = 3V

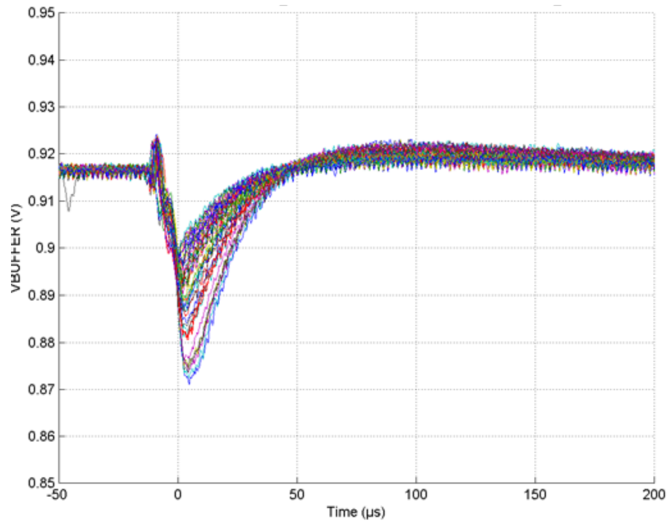


FIGURE 31. BUFFER COMPOSITE SET PLOT, RUN 211, V_{IN} = 3V

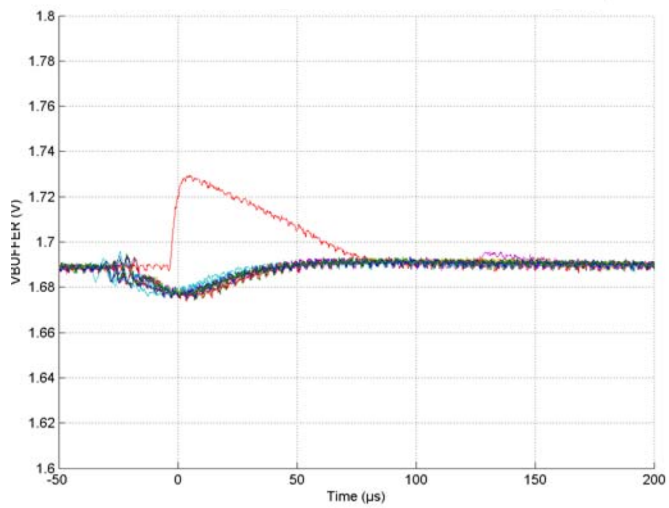


FIGURE 32. BUFFER COMPOSITE SET PLOT, RUN 215, V_{IN} = 13.2V

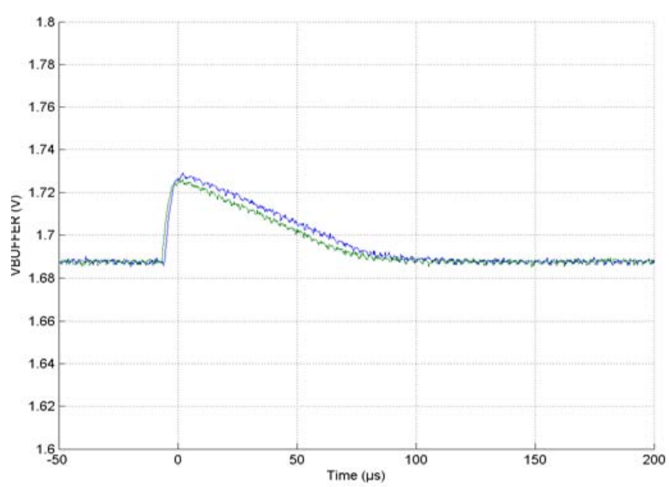


FIGURE 33. BUFFER COMPOSITE SET PLOT, RUN 217, V_{IN} = 13.2V

Figure 34 is the composite plot of the 50 first captures of run 222. The buffer is resistively loaded with 62.5Ω. Once again the SETs are in the negative direction.

In all conditions the response is controlled without oscillations to the output of the buffer amplifier. Typical DDR memory power solutions will have 20 times the amount of capacitive loading, which will mitigate SET. In addition, V_{REF} is an input to a differential pair, common-source amplifier, so there will be no significant current draw, which SEE testing has demonstrated will result in a very small SET cross section.

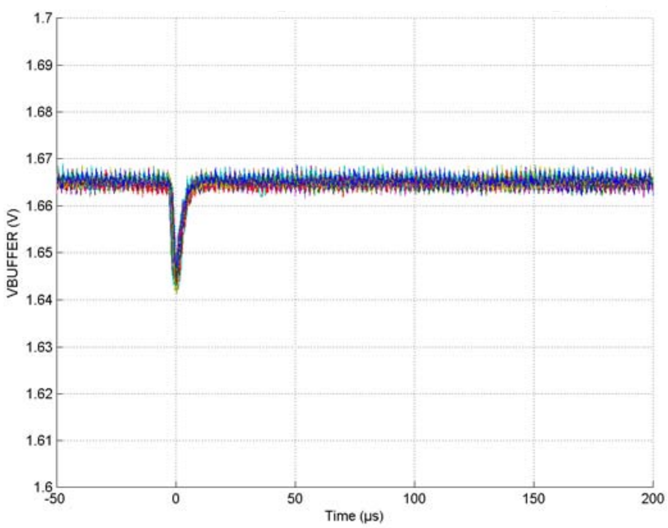


FIGURE 34. BUFFER COMPOSITE SET PLOT, RUN 222, V_{IN} = 13.2V

Summary

Destructive SEE

No SEL/SEB/SEGR was observed for the device up to an LET of 86.4MeV•cm^2/mg (+125°C) at a maximum voltage supply of V_{IN} = 14.7V when the DUT is disabled or sourcing to the maximum rated load current, providing over 10% margin to the maximum recommended input voltage of 13.2V.
Applications that result in a negative inductor valley current are limited to maximum voltage supply of V_{IN} = 13.7V, a 3% margin to the maximum recommended input voltage of 13.2V. In DDR applications typical input voltages are from 3.3V or 5V rails and 13.7V provides more than enough headroom to use this device as a V_{TT} termination regulator.

Single Event Transient

Even though complete triple redundancy is not employed in the control loop, the ISL70003SEH provides excellent single event transient response and we have met our goal of <3% deviation. Further mitigation of the transient may be used by increasing the amount of capacitance on the output filter. Testing has been conducted with a single 150µF tantalum output capacitor.

The SEFI phenomenon is still seen on the regulator with 3V input voltage at LET 86.4MeV•cm^2/mg only and the cross section is very small indicating a low probability of occurrence. Restart of the IC is autonomous with no outside intervention needed to return to normal operation. At a LET 60MeV•cm^2/mg the SEFIs go away with 3V input. SEFIs are not seen with input voltages above 5.5V at LET 86.4MeV•cm^2/mg.

Additional SET has been done on the buffer amplifier and current monitor. Both outputs demonstrate a controlled response due to an ion strike with no oscillations.

References

[1] JEDEC STANDARD JESD8-9A. Stub Series Terminated Logic for 2.5V (SSTL_2)

[2] Intersil Web-based report, 'Single Event Effects (SEE) Testing of the ISL70002SEH Synchronous Buck Regulator'.

[3] Intersil Web-based report, 'Single Event Effects (SEE) Testing of the ISL70001SRH Synchronous Buck Regulator'.

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