ISL71831SEH

Neutron Testing of the ISL71831SEH 32-Channel Analog Multiplexer

Introduction

This report summarizes results of 1MeV equivalent neutron testing of the ISL71831SEH 32-channel low voltage analog multiplexer. The test was conducted to determine the sensitivity of the part to displacement damage (DD) caused by neutron or proton environments. Neutron fluences ranged from 5×10^{11}n/cm^2 to 1×10^{13}n/cm^2.

Product Description

The ISL71831SEH is a radiation tolerant 32-channel analog multiplexer that is fabricated using Renesas proprietary P6SOI process technology to provide excellent latch-up performance. The part operates over a single supply range from 3V to 5.5V and has five digital address inputs and an enable pin that can be driven with adjustable logic thresholds to select one of 32 available channels. Inactive channels are isolated from the active channel by high impedance, which inhibits any interaction between them.

The low switch ON-resistance of the ISL71831SEH allows for improved signal integrity and reduced power losses. The part is also designed for cold sparing, making it compatible with redundancy techniques in high reliability applications. It provides a high impedance to the analog source in a powered OFF condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71831SEH also has analog overvoltage protection on the switch inputs that disables the switch during an overvoltage event to protect upstream and downstream devices. All inputs are electrostatic discharge (ESD) protected to 5kV Human Body Model (HBM).

The ISL71831SEH is available in a 48 Ld ceramic Quad Flatpack (CQFP) and operates across the extended temperature range of -55°C to +125°C.

A typical application schematic for the ISL71831SEH is shown in Figure 1.

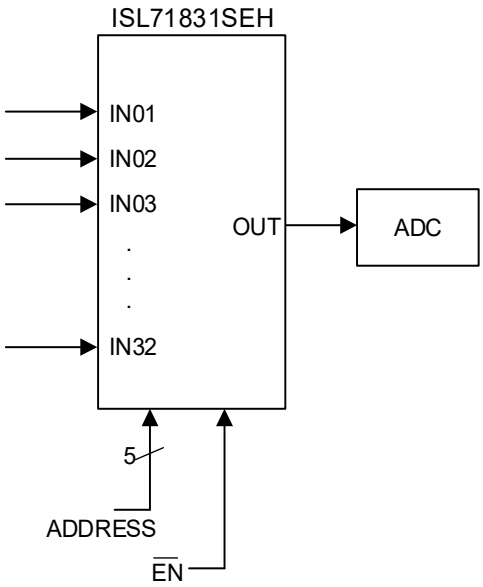

Figure 1. ISL71831SEH Typical Application Schematic

© 2022 Renesas Electronics

Contents

1. Test Description 3
1.1 Irradiation Facility 3
1.2 Test Fixturing 3
1.3 Radiation Dosimetry 3
1.4 Characterization Equipment and Procedures 3
1.5 Experimental Matrix 3
2. Results 4
2.1 Attributes Data 4
2.2 Variables Data 4
3. Discussion and conclusion 16
4. Revision History 16
Appendix 17

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on August 31, 2021, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were 5×10^{11}n/cm^2, 2×10^{12}n/cm^2, and 1×10^{13}n/cm^2. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cool-down time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 1. ISL71831SEH Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm^2)	Reactor Power (kW)	Time (s)	Fluence Rate (n/cm^2-s)[1][2]	Gamma Dose (rad(Si))[3]	Measured Fluence (n/cm^2)[4]
CRF#62106-A	5.00E+11	10	617	8.10E+08	70	5.38E+11
CRF#62106-B	2.00E+12	100	247	8.10E+09	281	2.05E+12
CRF#62106-C	1.00E+13	1000	123	8.10E+10	1401	1.14E+13

1. Dosimetry method: ASTM E-265.
2. The neutron fluence rate is determined from Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell (6/18/02). Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41krad(Si)/hr ±5.3% as mapped by TLD-based dosimetry.
4. Validated by S-32 flux monitors

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples irradiated at 5×10^{11}n/cm^2, five to be irradiated at 2×10^{12}n/cm^2, and five to be irradiated at 1×10^{13}n/cm^2. The actual levels achieved, which are shown in Table 2, were 5.38×10^{11}n/cm^2, 2.05×10^{12}n/cm^2, and 1.14×10^{13}n/cm^2. Five control units were used.

The 15 ISL71831SEH samples were drawn from Lot 5STWBEH. Samples were packaged in the 48Ld Ceramic Quad Flatpack (CDFP) production package. Samples were processed through burn-in before irradiation and were screened to the SMD limits at room, low, and high temperatures before the start of neutron testing.

2. Results

Neutron testing of the ISL71831SEH is complete, and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is not total dose testing, where the damage is cumulative.

2.1 Attributes Data

Table 2. ISL71831SEH Attributes Data

1MeV Fluence, (n/cm^2)		Sample size	Pass[1]	Fail	Notes
Planned	Actual				
5×10^{11}	5.38×10^{11}	5	5	0	Most passed[2]
2×10^{12}	2.05×10^{12}	5	5	0	All passed
1×10^{13}	1.14×10^{13}	5	5	0	All passed

1. A pass indicates a sample that passes all SMD limits.
2. One sample experienced data corruption and was removed from switch ON-resistance match (Figure 3), Break-Before-Make delay (Figure 21), and enable OFF to multiplexer output propagation delay (Figure 23) measurements.

2.2 Variables Data

The plots in Figure 2 through Figure 23 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible because of their values compared to the scale of the graph. While the applicable electrical limits taken from the SMD are also shown, it should be noted that these limits are provided for guidance only as the ISL71831SEH is not specified for the neutron environment.

All samples passed the post - TID irradiation SMD limits after all three exposures up to and including $1.14\times10^{13}n/cm^2$. One sample that was exposed to $5.38\times10^{11}n/cm^2$ experienced data corruption of three parameter measurements either during test datalogging or transferring the data to a spreadsheet, and those data points were removed from the switch ON-resistance match (Figure 3), Break-Before-Make delay (Figure 21), and enable OFF to multiplexer output propagation delay (Figure 23) measurements.

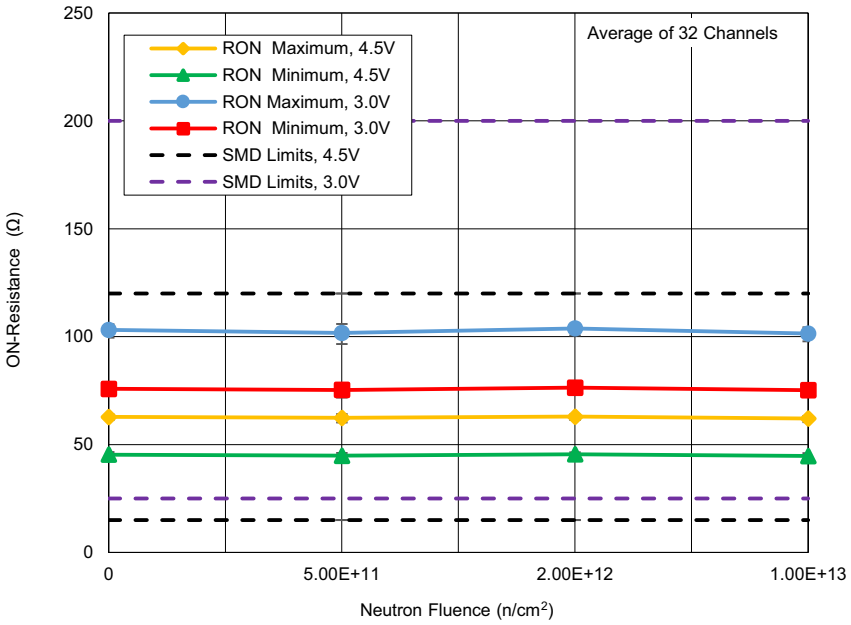

Figure 2. ISL71831SEH minimum and maximum switch ON-resistance average of all 32 channels with V^+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of 15Ω with a maximum 120Ω for supply voltage of 4.5V, and a minimum of 25Ω with a maximum 200Ω for supply voltages of 3.0V.

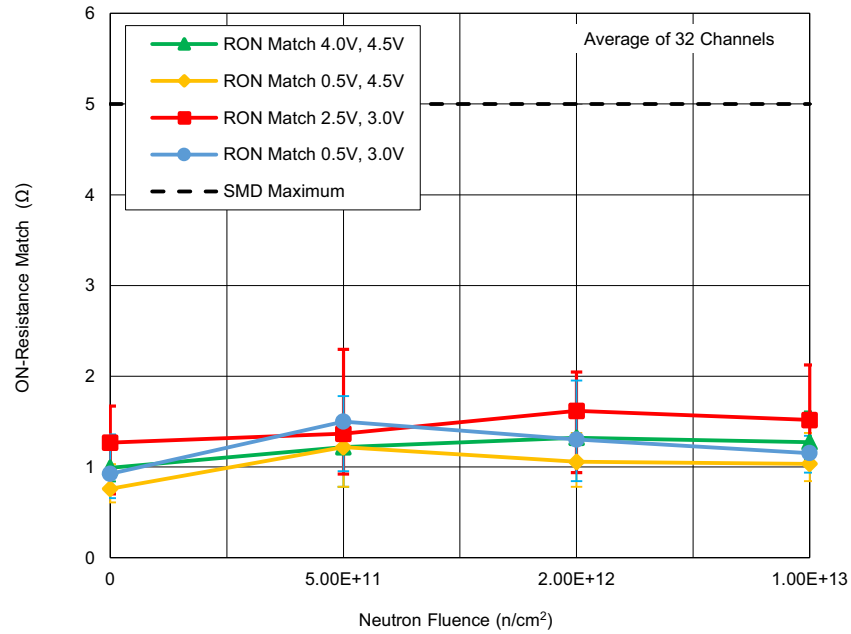

Figure 3. ISL71831SEH switch ON-resistance match average of all 32 channels with V^+ = 4.5V and V_{IN} = 4.0V and 0.5V or V^+ = 3.0V and V_{IN} = 2.5V and 0.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limit is a maximum of 5Ω for both supply voltages.

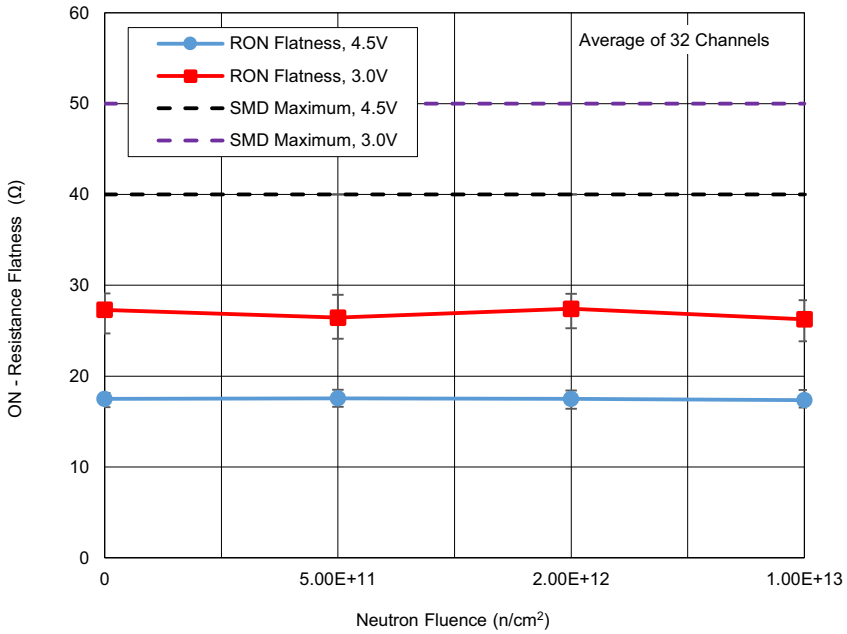

Figure 4. ISL71831SEH ON-resistance flatness average of all 32 channels with V^+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are maximums of 40Ω for a 4.5V supply voltage, and 50Ω for a 3.0V supply voltage.

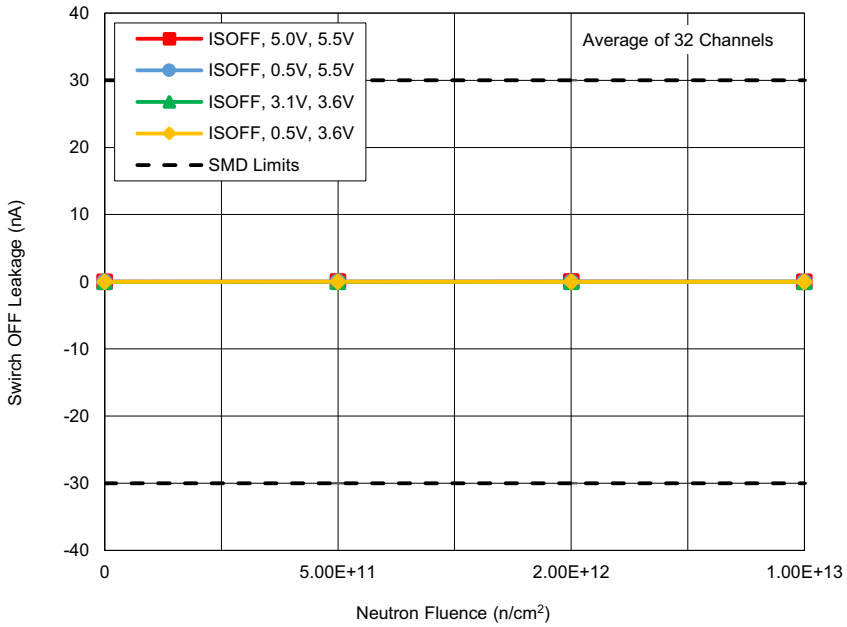

Figure 5. ISL71831SEH switch input OFF leakage average of all 32 channels with V^+ = 5.5V, V_{IN} = 5.0V, V_{OUT} = 0.5V, or V^+ = 5.5V, V_{IN} = 0.5V, V_{OUT} = 5.0V, or V^+ = 3.6V, V_{IN} = 3.1V, V_{OUT} = 0.5V, or V^+ = 3.6V, V_{IN} = 0.5V, V_{OUT} = 3.1V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of -30nA with a maximum of 30nA for both supply voltages.

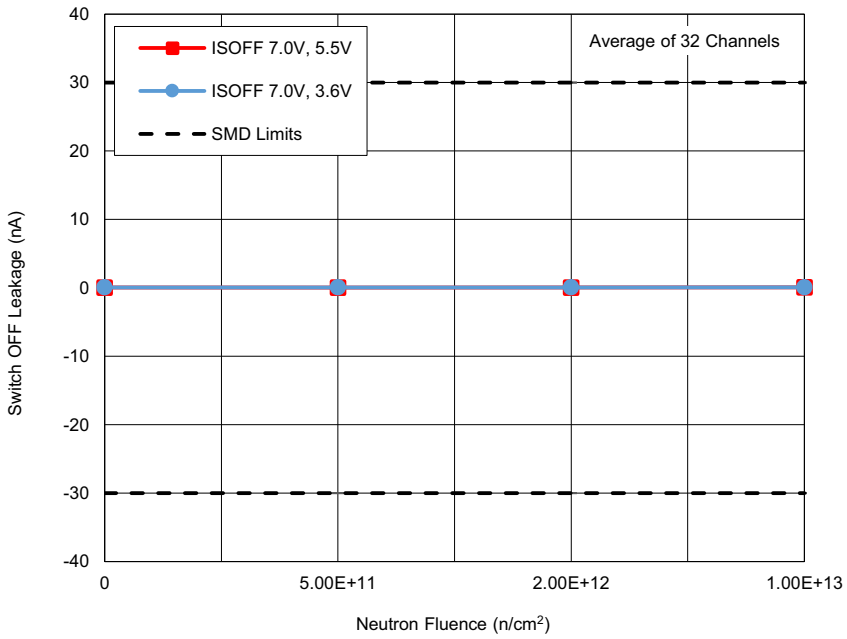

Figure 6. ISL71831SEH overvoltage switch input OFF leakage average of all 32 channels with V^+ = 5.5V, 3.6V, V_{IN} = 7.0V, and unused inputs and V_{OUT} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of -30nA with a maximum of 30nA for both supply voltages.

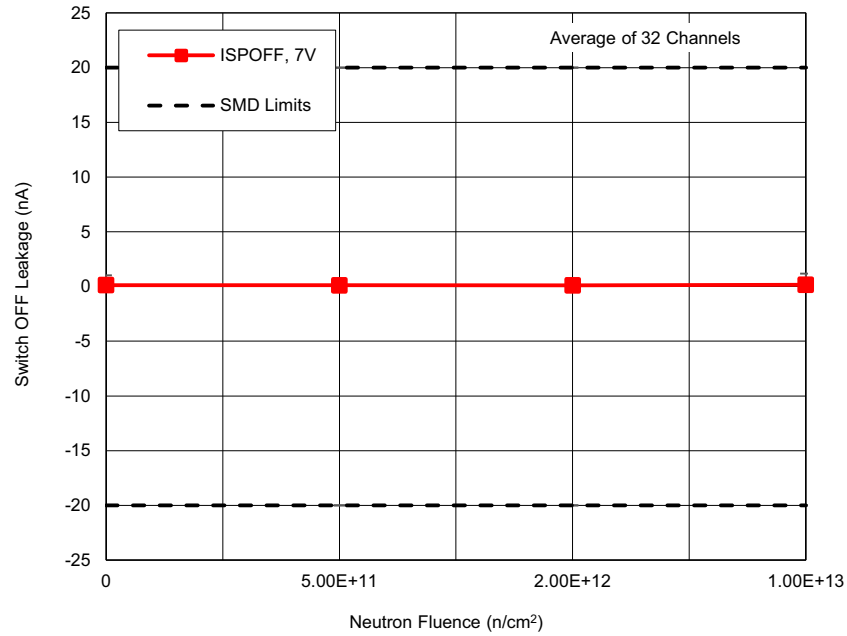

Figure 7. ISL71831SEH supply voltage grounded switch input OFF leakage into the input of an unselected channel average of all 32 channels with V_{IN} = 7V and V^+ = V_{OUT} = V_{EN} = V_{REF} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of -20nA with a maximum of 20nA.

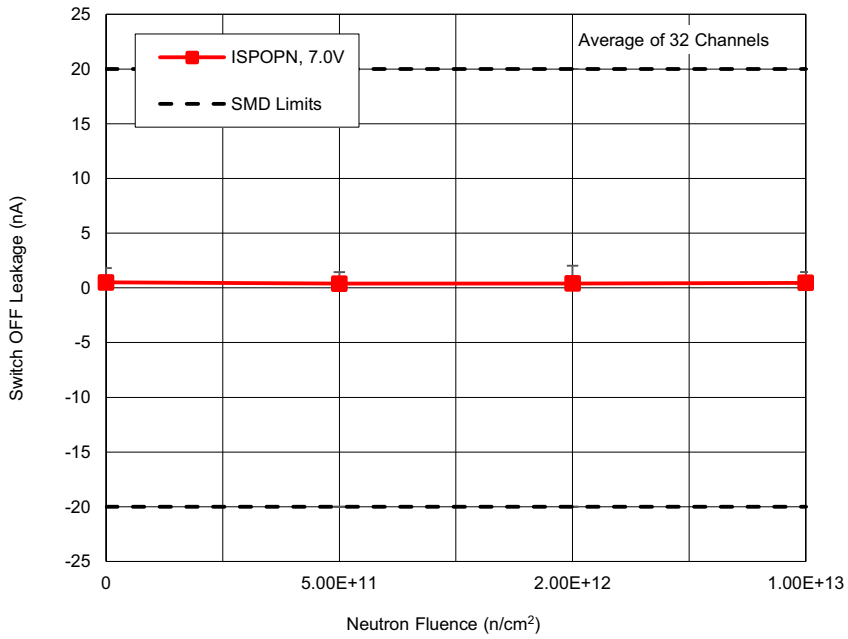

Figure 8. ISL71831SEH supply voltage open switch input OFF leakage into the input of an unselected channel average of all 32 channels with V_{IN} = 7V, V_{OUT} = 0V, and V^+ = V_{EN} = V_{REF} = Open following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of -20nA with a maximum of 20nA.

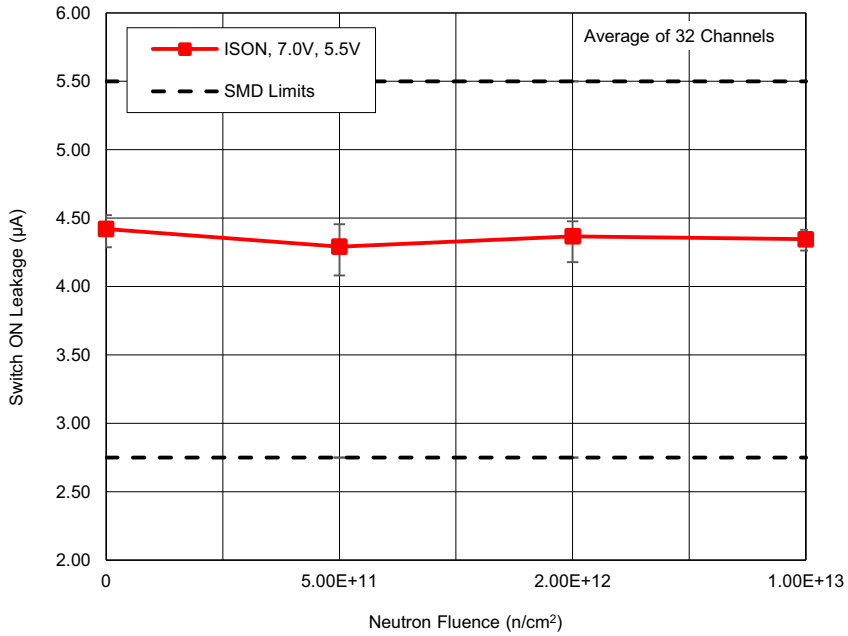

Figure 9. ISL71831SEH overvoltage switch ON input leakage into a selected channel average of all 32 channels with V^+ = 5.5V, V_{IN} = 7.0V, and V_{OUT} = Open following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of 2.75µA with a maximum of 5.50µA.

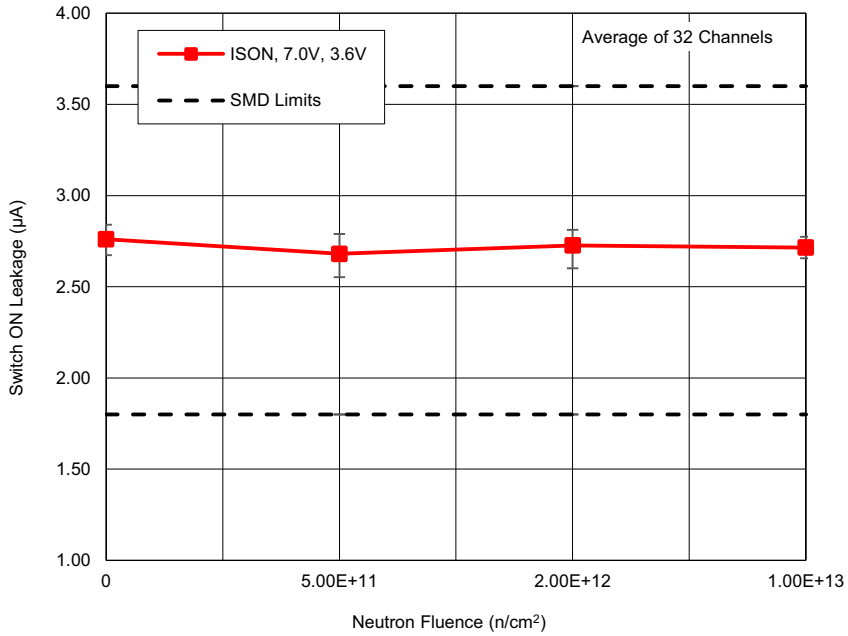

Figure 10. ISL71831SEH overvoltage switch ON input leakage into a selected channel average of all 32 channels with V^+ = 3.6V, V_{IN} = 7.0V, and V_{OUT} = Open following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of 1.8µA with a maximum of 3.6µA.

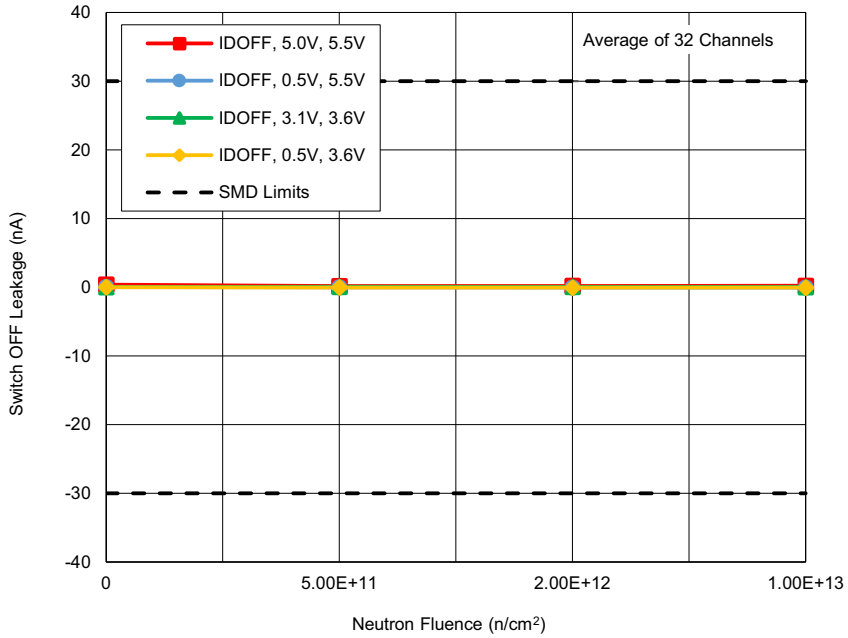

Figure 11. ISL71831SEH switch OFF leakage into the multiplexer output average of all 32 channels with V^+ = 5.5V, V_{IN} = 5.0V, V_{OUT} = 0.5V, or V^+ = 5.5V, V_{IN} = 0.5V, V_{OUT} = 5.0V, or V^+ = 3.6V, V_{IN} = 3.1V, V_{OUT} = 0.5V, or V^+ = 3.6V, V_{IN} = 0.5V, V_{OUT} = 3.1V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post – TID irradiation SMD limits are a minimum of -30nA with a maximum of 30nA for both supply voltages.

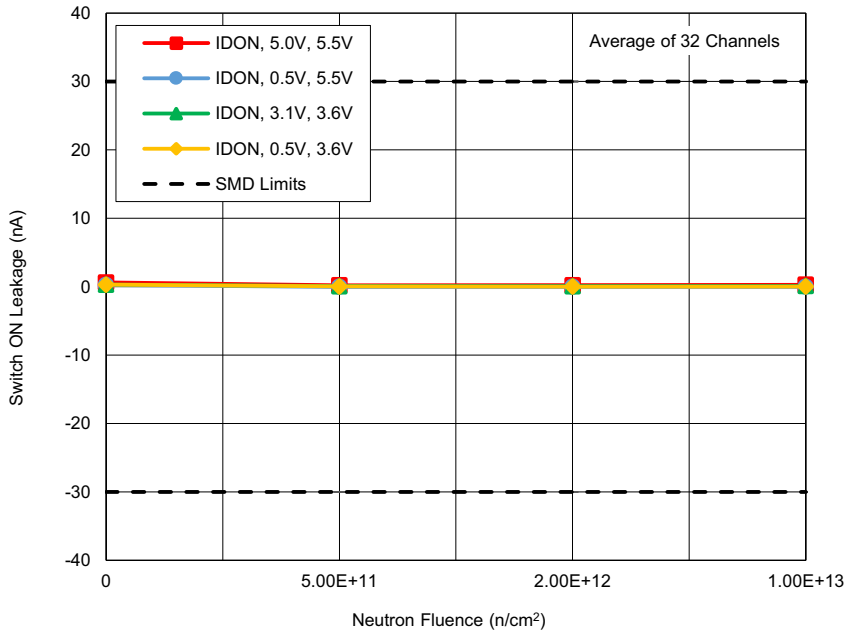

Figure 12. ISL71831SEH switch enabled switch leakage into the inputs and output for a selected switch average of all 32 channels with V^+ = 5.5V, V_{IN} = V_{OUT} = 5V, and all unused inputs at 0.5V, or V^+ = 5.5V, V_{IN} = V_{OUT} = 0.5V, and all unused inputs at 5V, or V^+ = 3.6V, V_{IN} = V_{OUT} = 3.1V, and all unused inputs at 0.5V, or V^+ = 3.6V, V_{IN} = V_{OUT} = 0.5V, and all unused inputs at 3.1V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all the channels. The post – TID irradiation SMD limits are a minimum of -30nA with a maximum for 30nA for both supply voltages.

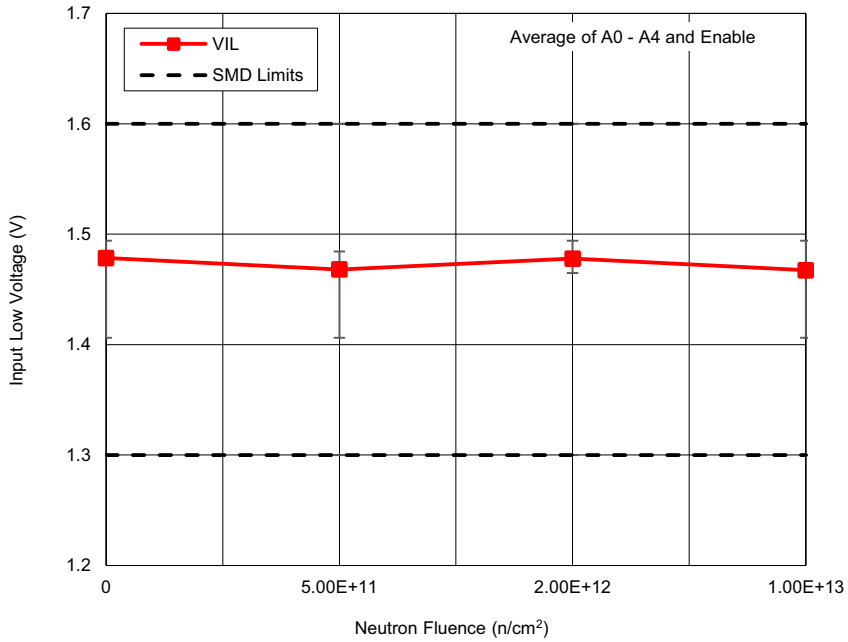

Figure 13. ISL71831SEH input LOW voltage average of address pins A0 through A3 and Enable pin following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post – TID irradiation SMD limits are a minimum of 1.3V with a maximum of 1.6V.

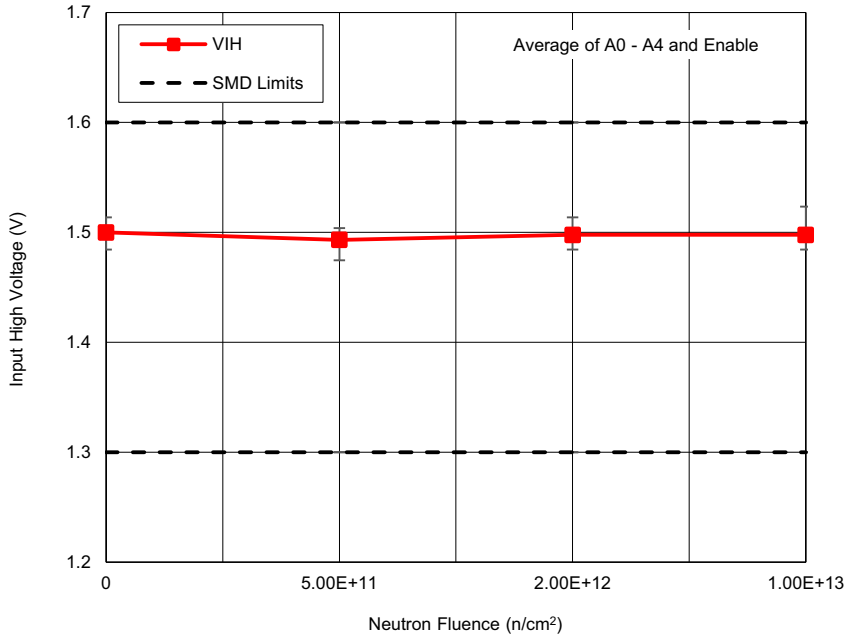

Figure 14. ISL71831SEH input HIGH voltage average of address pins A0 through A3 and Enable pin following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post – TID irradiation SMD limits are a minimum of 1.3V with a maximum of 1.6V.

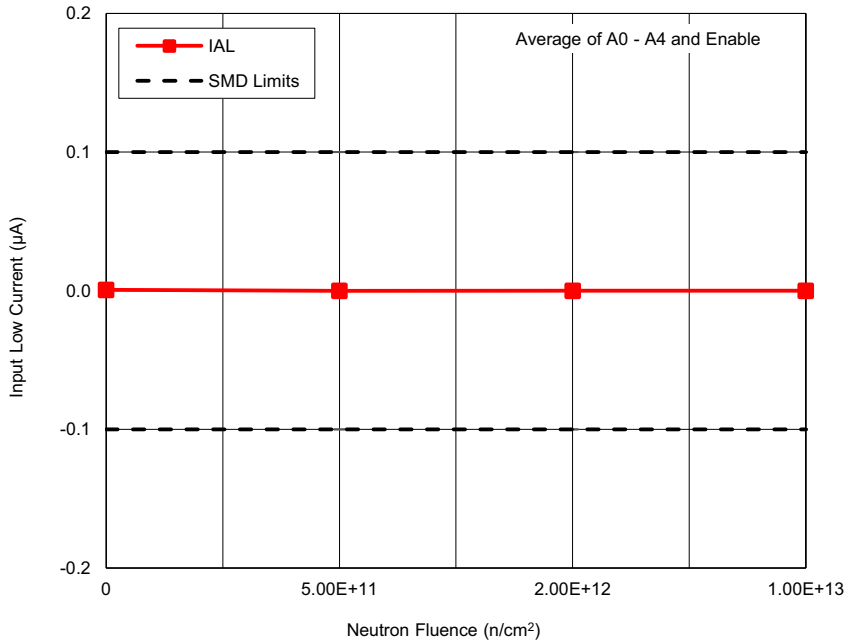

Figure 15. ISL71831SEH input LOW current average of address pins A0 through A3 and Enable pin following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post – TID irradiation SMD limits are a minimum of -0.1µA with a maximum of 0.1µA.

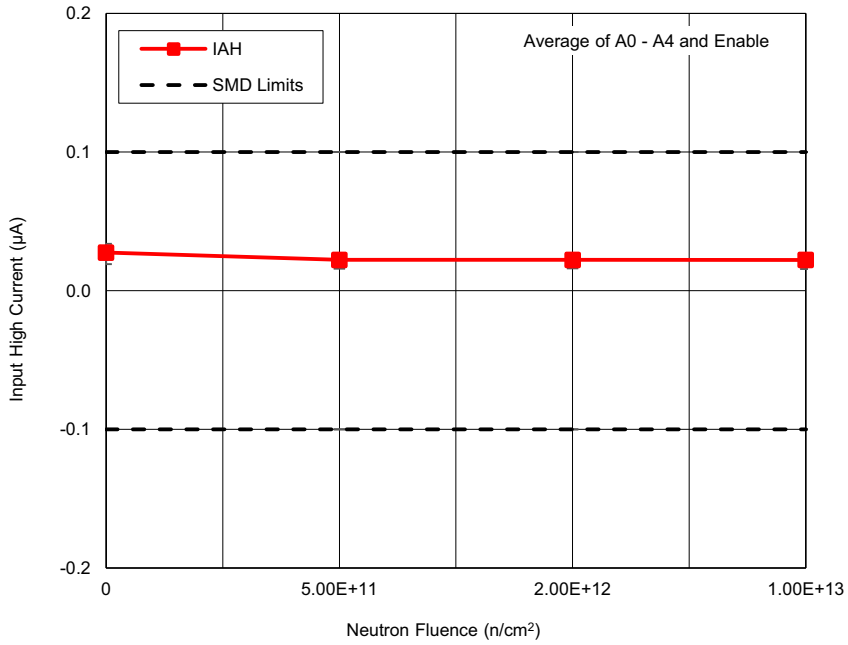

Figure 16. ISL71831SEH input HIGH current average of address pins A0 through A3 and Enable pin following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post – TID irradiation SMD limits are a minimum of -0.1µA with a maximum of 0.1µA.

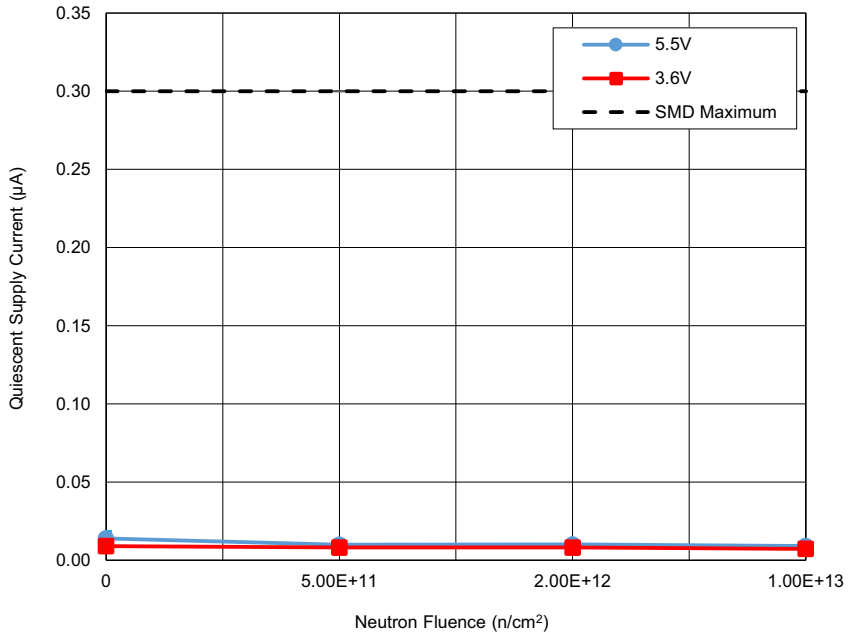

Figure 17. ISL71831SEH quiescent supply current with $V_+ = V_{REF}$ = 5.5V and 3.6V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post TID – irradiation SMD limit is a maximum of 0.3µA for both voltages.

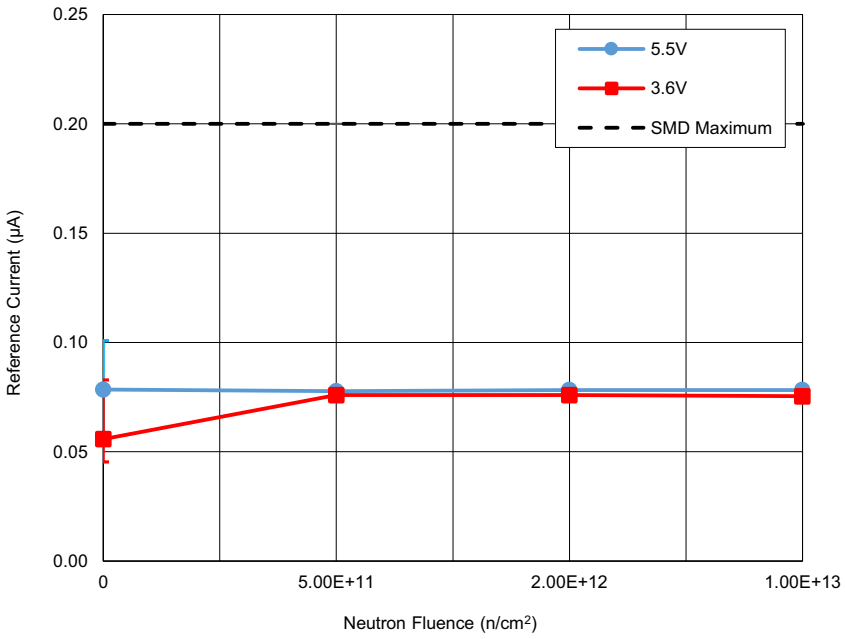

Figure 18. ISL71831SEH reference supply current with $V^+ = V_{REF}$ = 5.5V and 3.6V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post - TID irradiation SMD limit is a maximum of 0.2µA for both voltages.

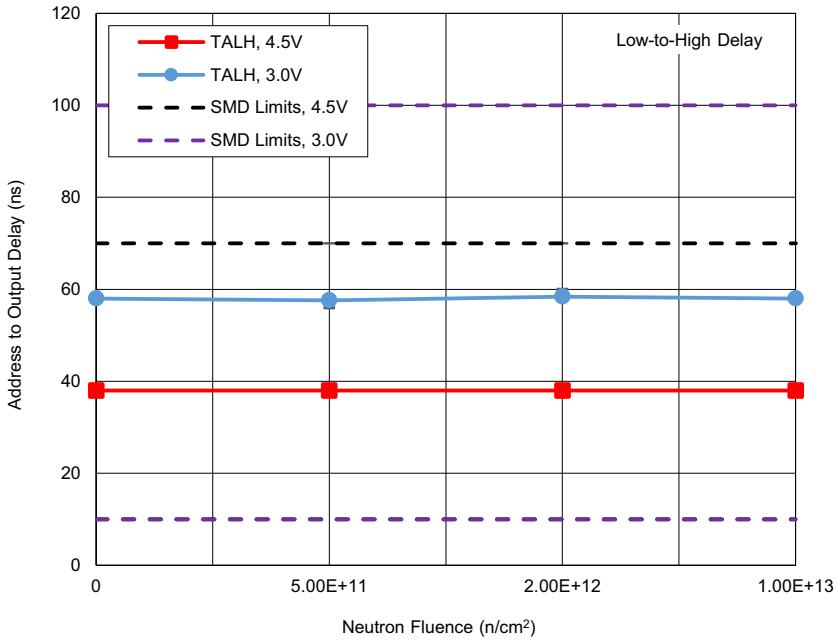

Figure 19. ISL71831SEH address input to multiplexer output delay (LOW to HIGH) with V^+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post – TID irradiation SMD limits are a minimum of 10ns with a maximum of 70ns for a 4.5V supply voltage and a minimum of 10ns with a maximum of 100ns for a 3.0V supply voltage.

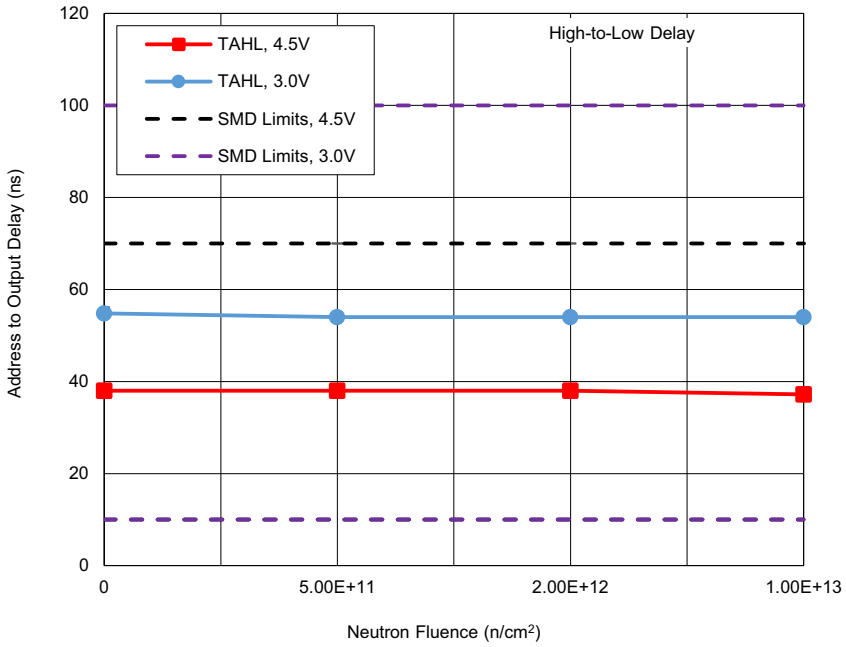

Figure 20. ISL71831SEH address input to multiplexer output delay (HIGH to LOW) with V^+ = 4.5V, 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post – TID irradiation SMD limits are a minimum of 10ns with a maximum of 70ns for a 4.5V supply voltage and a minimum of 10ns with a maximum of 100ns for a 3.0V supply voltage.

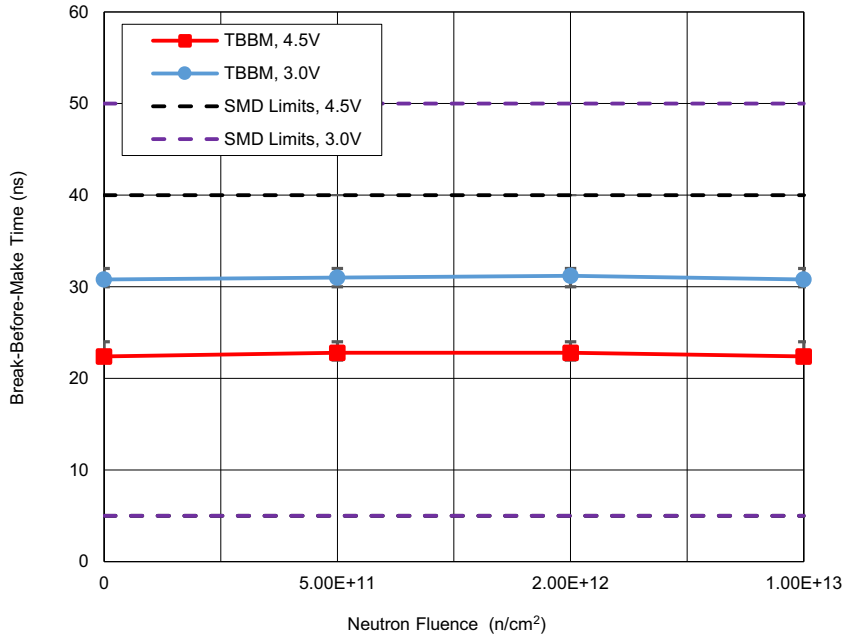

Figure 21. ISL71831SEH Break-Before-Make (BBM) delay with V^+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post – TID irradiation SMD limits are a minimum of 5ns with a maximum of 40ns for a 4.5V supply voltage and a minimum of 5ns with a maximum of 50ns for a 3.0V supply voltage.

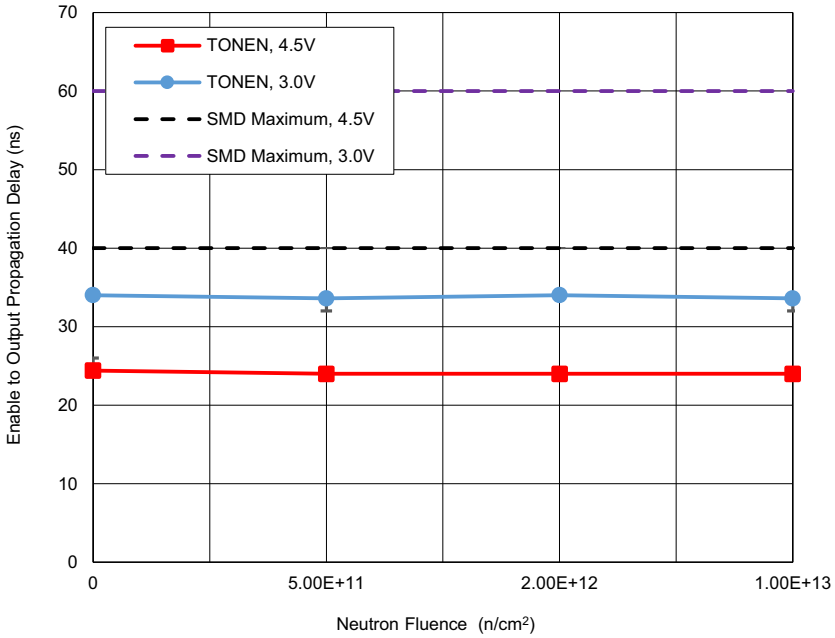

Figure 22. ISL71831SEH enable ON to multiplexer output propagation delay with V^+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post – TID irradiation SMD limits are maximums of 40ns for a 4.5V supply voltage and 60ns for a 3.0V supply voltage.

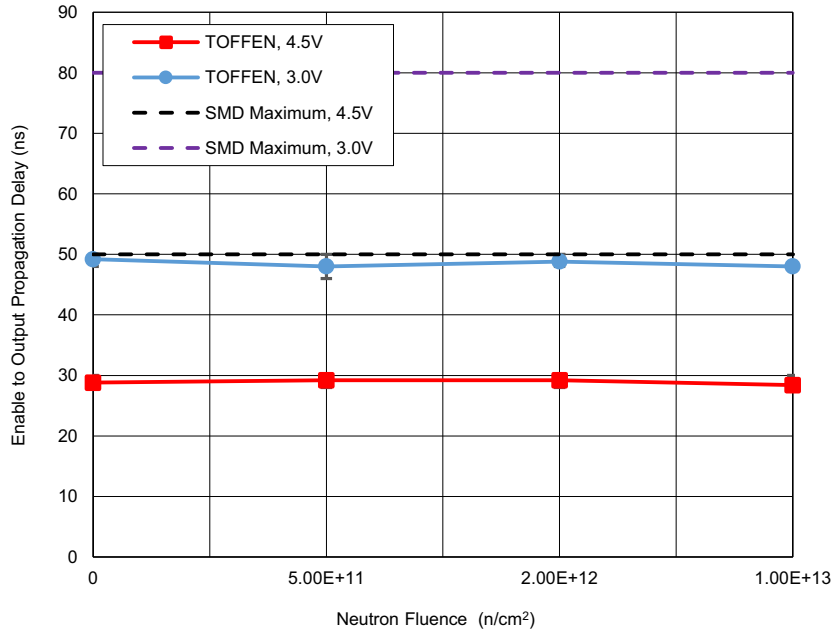

Figure 23. ISL71831SEH enable OFF to multiplexer output propagation delay with V^+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post – TID irradiation SMD limits are maximums of 50ns for a 4.5V supply voltage and 80ns for a 3.0V supply voltage.

3. Discussion and conclusion

This document reports the results of 1MeV equivalent neutron testing of the ISL71831SEH radiation tolerant 32-channel analog multiplexer. Parts were tested at actual fluences of 5.38×10^{11}n/cm^2, 2.05×10^{12}n/cm^2, and 1.14×10^{13}n/cm^2. The results of key parameters before and after irradiation to each level are plotted in Figure 2 through Figure 23. The plots show the mean of each parameter as a function of neutron irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD, but it should be noted that these limits are provided for guidance only as the ISL71831SEH is not specified for the neutron environment.

All samples passed the post - TID irradiation SMD limits after all three exposures up to and including 1.14×10^{13}n/cm^2. One sample that was exposed to 5.38×10^{11}n/cm^2 experienced data corruption of three parameter measurements either during test datalogging or transferring the data to a spreadsheet and those data were removed from the switch ON-resistance match (Figure 3), Break-Before-Make delay (Figure 21) and enable OFF to multiplexer output propagation delay (Figure 23) measurements.

4. Revision History

Revision	Date	Description
1.00	Aug 23, 2022	Initial release.

Appendix

Table 3. Reported Parameters

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
2	Channel On-Resistance	$r_{DS(ON)}$	V^+ = 3V, V_{IN} = 0V to V^+, I_{OUT} = 1mA	25	200	Ω
			V^+ = 4.5V, V_{IN} = 0V to V^+, I_{OUT} = 1mA	15	120	
3	$r_{DS(ON)}$ Match between Channels	$\Delta r_{DS(ON)}$	V^+ = 3V or 4.5V, V_{IN} = 0.5, I_{OUT} = 1mA	-	5	Ω
4	On-Resistance Flatness	$r_{FLAT(ON)}$	V^+ = 3.0V, V_{IN} = 0V to V^+	-	50	Ω
			V^+ = 4.5V, V_{IN} = 0V to V^+		40	
5	Switch Input Off Leakage	$I_{IN(OFF)}$	V^+ = 3.6V, V_{IN} = 3.1V or 0.5V, Unused inputs and V_{OUT} = 0.5V or 3.1V	-30	30	nA
			V^+ = 5.5V, V_{IN} = 5V or 0.5V, Unused inputs and V_{OUT} = 0.5V or 5V			
6	Switch Input Off Overvoltage Leakage	$I_{IN(OFF-0V)}$	V^+ = 3.6V or 5.5V, V_{IN} = 7V, Unused inputs and V_{OUT} = 0V	-30	30	nA
7	Switch Input Off Leakage with Supply Voltage Grounded	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V, $V^+ = V_{EN} = V_{REF}$ = 0V	-20	20	nA
8	Switch Input Off Leakage with Supply Voltage Open	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V, $V^+ = V_{EN} = V_{REF}$ = Open	-20	20	nA
9	Switch Input On Leakage with Overvoltage Applied to the Input	$I_{IN(ON-0V)}$	V^+ = 5.5V, V_{IN} = 7V, V_{OUT} = Open	2.75	5.5	µA
10			V^+ = 3.6V, V_{IN} = 7V, V_{OUT} = Open	1.8	3.6	
11	Switch Output Off Leakage	$I_{OUT(OFF)}$	V^+ = 3.6V, V_{OUT} = 3.1V or 0.5V, All inputs at 0.5V or 3.1V	-30	30	nA
			V^+ = 5.5V, V_{OUT} = 5V or 0.5V, All inputs at 0.5V or 5V			
12	Switch Output On Leakage with Switch Enabled	$I_{OUT(ON)}$	V^+ = 3.6, $V_{IN} = V_{OUT}$ = 3.1V or 0.5V, All unused inputs at 0.5V or 3.1	-30	30	nA
			V^+ = 5.5V, $V_{IN} = V_{OUT}$ = 5V or 0.5, All unused inputs at 0.5V or 5V			
13	Logic Input Voltage Low	V_{IL}	V^+ = 5.5V, V_{REF} = 3.3V	1.3	1.6	V
14	Logic Input Voltage High	V_{IH}	V^+ = 5.5V, V_{REF} = 3.3V	1.3	1.6	V
15	Logic Input Current Low	I_{AL}, I_{ENL}	V^+ = 5.5V, V_{REF} = 3.3V	-100	100	nA
16	Logic Input Current High	I_{AH}, I_{ENH}	V^+ = 5.5V, $V_{EN} = V_A = V_{REF}$	-100	100	nA
17	Quiescent Supply Current	I_{SUPPLY}	$V^+ = V_{REF} = V_{EN}$ = 3.6V or 5.5V	-	0.3	µA
18	V_{REF} Supply Current	I_{REF}	$V^+ = V_{REF} = V_{EN}$ = 3.6V or 5.5V, V_A = 0V	-	0.2	µA
19	Addressing Transition Time (Low to High)	t_{ALH}	V^+ = 3V	10	100	ns
			V^+ = 4.5V		70	
20	Addressing Transition Time (High to Low)	t_{AHL}	V^+ = 3V	10	100	ns
			V^+ = 4.5V		70	
21	Break-Before-Make Delay	t_{BBM}	V^+ = 3V	5	50	ns
			V^+ = 4.5V		40	

Table 3. Reported Parameters (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
22	Enable Turn-On Time	$t_{EN(ON)}$	V^+ = 3V	-	60	ns
			V^+ = 4.5V		40	
23	Enable Turn-Off Time	$t_{EN(OFF)}$	V^+ = 3V	-	80	ns
			V^+ = 4.5V		50	

Related Information

For a full list of related documents, visit our website:

- ISL71831SEH device page
- MIL-STD-883 test method 1017

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.