

Smart Configurator for RL78 Plug-in in e² studio 2023-07 Smart Configurator for RL78 V1.7.0

Release Note

Introduction

Thank you for using the Smart Configurator for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

Smart Configurator for RL78 V1.7.0 is equivalent to Smart Configurator for RL78 Plug-in in e² studio 2023-07.

1.1 System Requirements

The operating environment is as follows.

1.1.1 Windows PC

- System: x64/x86 based processor
 - Windows® 11

Windows® 10 (64-bit version)

- Windows® 8.1 (64-bit version)
- Memory capacity: We recommend 4 GB or more.
- Capacity of hard disk: At least 300 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

1.1.2 Linux PC

Smart Configurator for RL78 plug-in in e² studio 2023-01 or later is supported on Linux OS.

• System: x64 based processor, 2 GHz or faster (with multicore CPUs)

Ubuntu 22.04 LTS Desktop (64-bit version) Ubuntu 20.04 LTS Desktop (64-bit version)

- Memory capacity: We recommend 2 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

1.1.3 Development Environments

- Renesas Electronics Compiler for RL78 [CC-RL] V1.12 or later
- LLVM for Renesas RL78 10.0.0.202209 or later
- IAR Embedded Workbench for Renesas RL78 V5.10.1 or later
- SMS Assembler Note1 V1.00.00 or later
- FAA Assembler Note2 V1.04.02 or later

Note:

1. If you want to add SMS Assembler to e^2 studio, install it from the integrated installer of e^2 studio 21-04 or later. (e^2 studio)

As with other compilers, select and install from the [Additional Software] - [Renesas Toolchains & Utilities] tab of the e² studio setup wizard.

2. If you want to add FAA Assembler to e^2 studio, install it from the integrated installer of e^2 studio 23-04 or later. (<u>e² studio</u>)

As with other compilers, select and install from the [Additional Software] - [Renesas Toolchains & Utilities] tab of the e² studio setup wizard.



2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.7.0.

Table 2-1 Support Devi	ces (1/2)	
Group (HW Manual number)	PIN	Device name
RL78/G23 Group	30pin	R7F100GAFxSP, R7F100GAGxSP, R7F100GAHxSP, R7F100GAJxSP
(R01UH0896EJ0120)	32pin	R7F100GBFxNP, R7F100GBGxNP, R7F100GBHxNP, R7F100GBJxNP,
	Szpin	R7F100GBFxFP, R7F100GBGxFP, R7F100GBHxFP, R7F100GBJxFP
	36pin	R7F100GCFxLA, R7F100GCGxLA, R7F100GCHxLA, R7F100GCJxLA
	40pin	R7F100GEFxNP, R7F100GEGxNP, R7F100GEHxNP, R7F100GEJxNP
	44pin	R7F100GFFxFP, R7F100GFGxFP, R7F100GFHxFP, R7F100GFJxFP,
	•	R7F100GFKxFP, R7F100GFLxFP, R7F100GFNxFP
	48pin	R7F100GGFxFB, R7F100GGGxFB, R7F100GGHxFB, R7F100GGJxFB, R7F100GGKxFB, R7F100GGLxFB, R7F100GGNxFB, R7F100GGFxNP, R7F100GGGxNP, R7F100GGHxNP, R7F100GGJxNP, R7F100GGKxNP, R7F100GGLxNP, R7F100GGNxNP
	52pin	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA, R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
	64pin	R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB, R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB, R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxLA, R7F100GLGxLA, R7F100GLHxLA, R7F100GLJxLA, R7F100GLKxLA, R7F100GLLxLA, R7F100GLNxLA
	80pin	R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA, R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB, R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	100pin	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB, R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA, R7F100GPJxFA, R7F100GPKxFA, R7F100GPLxFA, R7F100GPNxFA
	128pin	R7F100GSJxFB, R7F100GSKxFB, R7F100GSLxFB, R7F100GSNxFB
RL78/F24 Group	32pin	R7F124FBJ3xNP, R7F124FBJ4xNP, R7F124FBJ5xNP
(R01UH0944EJ0100)	48pin	R7F124FGJ3xFB, R7F124FGJ4xFB, R7F124FGJ5xFB
	64pin	R7F124FLJ3xFB, R7F124FLJ4xFB, R7F124FLJ5xFB
	80pin	R7F124FMJ3xFB, R7F124FMJ4xFB, R7F124FMJ5xFB
	100pin	R7F124FPJ3xFB, R7F124FPJ4xFB, R7F124FPJ5xFB
RL78/G15 Group	8pin	R5F12008xNS, R5F12007xNS
(R01UH0959EJ0100)	10pin	R5F12018xSP, R5F12017xSP
	16pin	R5F12048xNA, R5F12047xNA, R5F12048xSP, R5F12047xSP
	20pin	R5F12068xSP, R5F12067xSP
RL78/F23 Group	32pin	R7F123FBG3xNP, R7F123FBG4xNP, R7F123FBG5xNP
(R01UH0944EJ0100)	48pin	R7F123FGG3xFB, R7F123FGG4xFB, R7F123FGG5xFB
	64pin	R7F123FLG3xFB, R7F123FLG4xFB, R7F123FLG5xFB
	80pin	R7F123FMG3xFB, R7F123FMG4xFB, R7F123FMG5xFB
RL78/G22 Group	16pin	R7F102G4ExNP, R7F102G4CxNP
(R01UH0978EJ0100)	20pin	R7F102G6ExSP, R7F102G6CxSP
	24pin	R7F102G7ExNP, R7F102G7CxNP
	25pin	R7F102G8ExLA, R7F102G8CxLA
	30pin	R7F102GAExSP, R7F102GACxSP
	32pin	R7F102GBExNP, R7F102GBCxNP, R7F102GBExFP, R7F102GBCxFP
	36pin	R7F102GCExLA, R7F102GCCxLA
	40pin	R7F102GEExNP, R7F102GECxNP
	44pin	R7F102GFExFP, R7F102GFCxFP
	48pin	R7F102GGExFB, R7F102GGExNP, R7F102GGCxFB, R7F102GGCxNP

Table 2-1 Support Devices (1/2)



Group	PIN	Device name
(HW Manual number)		
RL78/G24 Group	20pin	R7F101G6GxSP, R7F101G6ExSP
(R01UH0961EJ0100)	24pin	R7F101G7GxNP, R7F101G7ExNP
	25pin	R7F101G8GxLA, R7F101G8ExLA
	30pin	R7F101GAGxSP, R7F101GAExSP
	32pin	R7F101GBGxNP, R7F101GBExNP, R7F101GBGxFP, R7F101GBExFP
	40pin	R7F101GEGxNP, R7F101GEExNP
	44pin	R7F101GFGxFP, R7F101GFExFP
	48pin	R7F101GGGxFB, R7F101GGExFB, R7F101GGGxNP, R7F101GGExNP
	52pin	R7F101GJGxFA, R7F101GJExFA
	64pin	R7F101GLGxFA, R7F101GLGxFB, R7F101GLExFA, R7F101GLExFB
RL78/G16 Group	10pin	R5F1211AxSP, R5F1211CxSP
(R01UH0980EJ0100)	16pin	R5F1214AxNA, R5F1214AxSP, R5F1214CxNA, R5F1214CxSP
	20pin	R5F1216AxSP, R5F1216CxSP
	24pin	R5F1217AxNA, R5F1217CxNA
	32pin	R5F121BAxFP, R5F121BAxNA, R5F121BCxFP, R5F121BCxNA



2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.7.0.

Table 2-3 Support Components (1/2)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
	12 Bit A/D Single Scan	-	-	✓	-	✓	-	-	-	
	12 Bit A/D Continuous Scan	-	-	✓	-	✓	-	-	-	
	12 Bit A/D Group Scan	-	-	1	-	1	-	-	-	
4		Normal mode	1	-	1	-	1	1		Only RL78/G24 A/D converter has mode selection GUI. For
		Advanced mode	-	-	-	-	-	-	1	other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
	Clock Output/Buzzer Output Controller	-	1	1	1	1	1	>	1	
6	Comparator	-	<	✓	✓	-	-	>	>	
	D/A Converter	-	~	✓	-	-	-	I	>	
	Data Transfer Controller	-	<	✓	-	~	<	I	>	
	Delay Counter	-	✓	1	1	1	✓	✓	✓	
	Divider Function	-	✓	✓	✓	✓	✓	✓	~	
	Event Link Controller	-	-	✓	-	-	✓	-	✓	
	External Event Counter	-	1	1	1	1	1	1	~	
	IIC Communication (Master mode)	-	1	~	1	1	~	1	1	
	IIC Communication (Slave mode)	-	1	~	1	1	~	1	1	
	Input Capture Function	-	-	1	-	1	-	-	1	
	Input Pulse Interval/Period Measurement	-	1	1	1	1	1	1	1	
	Input Signal High-/Low- Level Width Measurement	-	1	~	1	~	~	>	>	
	Interrupt Controller	-	✓	✓	✓	✓	✓	>	>	
19	Interval Timer	8 bit count mode	✓	1	1	1	✓	✓	✓	
		12 bit count mode	-	-	1	-	-	✓	-	
		16 bit count mode	✓	✓	✓	✓	✓	✓	~	
		16 bit capture mode	✓	-	-	-	✓	-	~	
		32 bit count mode	✓	-	-	-	✓	-	✓	
	Key Interrupt	-	✓	1	-	✓	1	-	1	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	✓	1	1	1	✓	✓	
		Two-Channel Input with One- Shot Pulse Output	-	-	1	-	-	1	-	
	Output Compare Function	-	-	1	-	1	-	-	✓	
	Ports	-	✓	✓	✓	✓	✓	✓	>	
	PWM Option Unit A	-	-	✓	-	✓	-	-	>	
	DALI Communication (Control devices)	-	_	_	_	-	-	-	1	
26	DALI Communication (Control gear)	-	-	-	-	-	-	-	1	
27	Real-Time Clock	-	✓	✓	-	✓	✓	1	✓	



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Table 2-4 Support Components (2/2) ✓: Support, -: Non-support RL78/G16 RL78/G24 RL78/G22 RL78/G23 RL78/F24 RL78/G15 **RL78/F23** No Components Mode Remarks 28 PWM Output PWM Mode 1 1 1 1 1 1 1 PWM3 Mode 1 1 1 _ _ _ _ Extended PWM Mode _ 1 1 _ 1 PWM2 Mode 1 _ _ Timer KB3 PWM Output Gate _ 1 _ _ _ _ Mode Standalone Mode (Period controlled by the TKBCRn0 _ 1 _ _ register) Standalone Mode (Period controlled by external trigger 1 input) Simultaneous Start/Stop Mode (Period controlled by _ _ _ 1 the TKBCRn0 register) Simultaneous Start/Stop Mode (Period controlled by _ 1 _ external trigger input) Simultaneous Start/Clear 2 3 3 3 3

		Mode (Period controlled by master)	-	-	-	-	-	-	1	
		Interleaved PFC Output Mode	-	-	-	-	-	-	1	
29	Remote Control Signal Receiver	-	1	-	-	-	-	-	-	
30	SNOOZE Mode Sequencer	-	<	-	-	-	✓	-	-	
31	SPI (CSI) Communication	Transmission	1	1	✓	1	✓	1	1	
		Reception	<	1	✓	1	✓	<	1	
		Transmission/reception	<	1	✓	1	✓	<	1	
32	Square Wave Output	-	<	1	✓	1	✓	<	1	
33	Three-phase PWM Output	Reset Synchronous PWM Mode	-	1	-	1	-	1	1	
		Complementary PWM Mode		1	-	1	-	<	1	
		Extended Complementary PWM Mode	-	1	-	1	-	1	1	
34	UART Communication	Transmission	<	1	✓	1	✓	<	1	
		Reception	<	✓	✓	1	1	<	✓	
		Transmission/reception	<	1	✓	1	✓	<	1	
35	Voltage Detector	-	1	1	-	1	✓	-	1	
36	Watchdog Timer	-	1	1	✓	1	✓	1	1	
37	Logic & Event Link Controller	-	1	-	-	-	-	-	-	Need download in Smart Configurator RL78
38	Phase Counting Mode	-	-	-	-	-	-	-	1	
39	Programmable Gain Amplifier	-	_	-	-	-	-	_	1	

Flexible Application

Accelerator

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2.3 New support

details.

2.3.1 Support RL78/G24 new components and modes

Support new components and modes about A/D Converter (Advanced mode), Digital Addressable Lighting Interface (DALI), 16-bit Timers KB30, KB31, and KB32 and Timer RD2. Please see Table 2-3 Support Components (1/2) Support Components (2/2) Support Components (2/2)

2.3.2 Support target board selection when creating Smart Configurator project in e² studio

From Smart Configurator for RL78 V1.7.0, the user can select more target boards except "Custom" in project generation wizard when creating Smart Configurator project in e² studio.

9	– 🗆 X
New Renesas CC-RL Executable Project	
Select toolchain, device & debug settings Toolchain Settings Language: © C C++ Toolchain: Renesas CC-RI	
Toolchain Version: V1.12.00 V Manage Toolchains	
Device Settings Target Board: Custom Custom Target Device: RL78G15_FastPrototypingBoard RL78G22_FastPrototypingBoard RL78G23-128p_FastPrototypingBoard RL78G23-64p_FastPrototypingBoard RL78G24_FastPrototypingBoard Project Type: Constant	Configurations ✓ Create Hardware Debug Configuration E1/E20 (RL78) ✓ Create Debug Configuration RL78 Simulator ✓ Create Release Configuration
? < Back	Next > Finish Cancel

Figure 2-1 Support target board selection



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2.3.3 Support blinky project generation

From Smart Configurator for RL78 V1.7.0, blinky project generation feature is supported. When the user selects target board file other than Custom in project generation wizard, Bare Metal - Blinky project template will be available and can be selected. After the user selected Bare Metal – Blinky project template, the generated project will implement blink LED resource for the selected target board.

	project template. nplate selection	1	_
0 🚺	Bare Metal - Minimal Bare metal project that includes BSP. This project will initialize clocks, pins, dr runtime environment.	ivers and	the (
•	Bare Metal - Blinky Bare metal project that includes BSP and will blink LED if available. This proje clocks, pins, drivers and C runtime environment.	ct will init	ialize

Figure 2-2 Bare Metal - Blinky project template selection

2.3.4 Support compare view for the user to resolve code confliction

If the merge conflict occurs, conflict message in red will be displayed in the Smart Configurator console, as shown in **Error! Reference source not found.**Figure 2-3 The conflict message and file compare view. The user can click the conflicted file in the console message to open the File Compare view as shown in Figure 2-3 The conflict message and file compare view and then can resolve the conflict.

g24 example.scfg	Compare view	
A Text Compare		
Existing code	 New code 	
<pre>/* Disable RTC clock operation */ RTCE = 00; /* Disable INTRTC interrupt */ RTCK = 00; /* Disable INTRTC interrupt */ RTCK = 00; /* Clear INTRTC interrupt flag */ RTCE = 00; /* Start user = 00 #TC_LL_32KH2; /* Set fRTCCK */ RTCCE = 00 #TC_LL_32KH2; /* Start user code */ POUS & extEd; /* End user code */ RTCCE = 00 #TC_LTAPLASHE = 00 #TC_12HOUR_MODE = 00 #TC_INTRTC_NOT_GENERATE); /* End user code */ RTCCE = 00; R_Config_RTC_Create_UserInit(); } Function Name: R_Config_HTC_Start * Description : This function enables the real-time clock. * Arguments : None * Return Value : None * Retur</pre>	RTCC0 = (_20.RTC.RTC.HT_EN /* Set alarm detect function WALE = 001; WALE = 001; /* Alarm function setting * AlARMAN = 00.RTC.ALARM MEN /* Set RTCHZ pin */ POX3 & 0xFEU; PX3 & 0xFEU; PX3 & 0xFEU; R_Config_RTC_Create_UserInit	*/ lag */ ALCE GORTCINTRTC_) */ ALCE GORTCINTRTCNOT_GENERATE); h t(); */
Console Sconfiguration Problems Smart Configurator Output	0 61 *	
M04050001: CNDW 0 is used for One shunt feature M04050001: CNDW 1 is used for One shunt feature M04050001: CNDW 2 is used for One shunt feature M000000001: Code generation is started	Confli	ct message
M04000001: File generated: <u>src\smc gen\Config RTC\Config RTC.c</u>		

Figure 2-3 The conflict message and file compare view

There are two methods to resolve the conflict:

Click button "Copy Current Change from Left to Right" and then delete unused code to resolve conflict.
 Resolve the conflict manually by copying the code in the left panel to the right panel or editing the code in the right panel directly.

Note: After confliction resolved, if click the conflict message, it still opens compare view.



2.3.5 Support symbolic name in Pin configuration

From Smart Configurator for RL78 V1.7.0, new feature to define symbolic name is supported in [Pin number] view. By defining the user's own symbol for multiplex pin, user can maintain same software even if the MCU is changed. The symbolic name can be migrated when changing device only on condition that the pin with symbolic name is assigned. The symbolic name macro is generated in file pin.h when generating code.

Pin Number							24
type filter tex	t (* = any string, ? = any charac	ter)				All	~
Pin Numb	Pin Name	Board Func	Function	Direction	Remarks	Symbolic Name	Cor ^
1	P142/SCK30/SCL30		SCK30	IO	There is no softwar	SW1	
2	P141/PCLBUZ1/INTP7		Not assigned	None			
3	P140/PCLBUZ0/INTP6		INTP6	I	There is no softwar	SW2	
4	P120/ANI19/IVCMP1/EI120		Not assigned	None			
E	D07/ANI01		New Contractor	News	-		

Figure 2-4 Symbolic name setting

⊕Macro definitions									
⊖/* User's guide for symbolic name.									
* The generated symbolic names can be used in the user application as follows:									
*									
* Example: Toggle LED1 at Pin P54.									
* There are 2 ways to toggle LED1 User guide, always generate									
* 1) Using symbolic name macro									
* Assuming the symbolic name for P54 is "LED1", the generated macro definition will be:									
* #define LED1 5,4									
*									
* To use this macro definition to toggle the LED1, call the symbolic name APIs:									
<pre>* PIN_WRITE(LED1) = ~PIN_READ(LED1)</pre>									
*									
* 2) Not using symbolic name macro									
* Call the symbolic name APIs directly									
<pre>* PIN_WRITE(5,4) = ~PIN_READ(5,4)</pre>									
*/									
(* C * /									
/* Symbolic name */ #define SW1 14.2 Symbolic name generated when generating each									
#define SW1 14,2 Symbolic name generated when generating code									
/* Pin write helper */									
<pre>#define PIN WRITE HELPER(x,y) ((P##x## bit.no##y))</pre>									
/* Pin read helper */									
<pre>#define PIN READ HELPER(x,y) ((P##x## bit.no##y))</pre>									
/* Pin write API */ #define PIN_WRITE() Symbolic name API, always generate (PIN WRITE HELPER(_VA_ARGS_))									
/* Pin read API */									
#define PIN_READ() (PIN_READ_HELPER(VA_ARGS))									

Figure 2-5 Code in pin.h



✓: Applicable, -: Not Applicable

3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.7.0.

3.1 Correction of issues/limitations

Table 3-1 List of Correction of issues/limitations

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Fixed the issue of build warning about security option byte in CC-RL V1.12	-	~	-	1		-	-	

3.1.1 Fixed the issue of build warning about security option byte in CC-RL V1.12

In CS+, when the CC-RL compiler version is V1.12, there is a build warning W0561520 about security option byte. This issue has been fixed from Smart Configurator for RL78 V1.7.0.

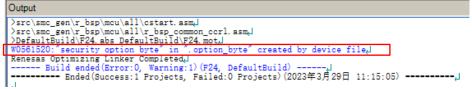


Figure 3-1 CC-RL V1.12 build warning

[On-chip debug and flash serial programming security ID reading setting] is added on System page. After generating code, the property of CC-RL (Build tool) will change according to the user's setting. When "Unuse" is selected, "Security option byte value" is FA. When "Use" is selected, "Security option byte value" is FE.

○ Unused	Use emulator	○ COM Port	
Security ID authentication	failure setting		
⊖ Do not erase flash men	nory data		
Security ID authentication O Do not erase flash men Erase flash memory dat On-chip debug and flash	nory data	g setting	

Figure 3-2 On-chip debug and flash serial programming security ID reading setting

~	Device	
	Set enable/disable on-chip debug by link option	Yes(-OCDBG)
	Option byte values for OCD	HEN A4
	Set security option byte	Yes(-SECURITY_OPT_BYTE)
	Security option byte value	HEX FE
1	Set debug monitor area	Yes(Specify address range)(-D
	Range of debug monitor area	1FE00-1FFFF
	Set user option byte	Yes(-USER_OPT_BYTE)
	User option byte value	HEX EFE3E0
	Control allocation to trace RAM area	Yes(Error message)(-OCDTR)
	Control allocation to hot plug-in RAM area	No
/	Output Code	
Sel	ecify execution start address ect whether to specify the execution start address s option corresponds to the -ENTry option of the rl	

Figure 3-3 Set CS+ property about security option byte



3.2 **Specification changes**

Table 3-2	List of	Specification	changes
-----------	---------	---------------	---------

Tab	Table 3-2 List of Specification changes ✓ : Applicable, -: Not Applic					e, -: Not Applicable			
No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Improvement for adding the user code area at the end of the interrupt function of input capture function	-	1	-	1	_	-	~	
2	Improvement for Internal reference voltage can be used when VDD ≥ 2.4V in Comparator	-	-	1	-	-	1	-	
3	mprovement for Internal reference voltage can be used when VDD ≥ 2.4V in A/D converter	-	-	1	-	-	1	-	
4	Improvement for adding PMC setting for INTP and TAU pins' setting	-	-	-	-	-	1	-	
5	Improvement for the specification according to RL78G16 UM from V0.9 to V1.0	-	-	-	-	-	1	-	
6	Improvement for the specification according to RL78G24 UM from V0.8 to V1.0	-	-	-	-	-	-	1	
7	Improvement for adding include path to build setting by default after code generation	1	1	1	1	1	1	1	

Improvement for adding the user code area at the end of the interrupt function of 3.2.1 input capture function

When using the input capture function of timer (the function to measure the input signal), in most cases, the user adds the code to set the flag to know the capture completion. So, Smart Configurator adds the user code area in the interrupt function. The following is an example by using TRG input capture function.

```
void r_TRG_input_interrupt(void)
1
    uint8_t trgier_temp = TRGIER0;
uint32_t temp;
    TRGIER0 = 0 \times 000U;
     if ((TRGSR0 & _08_TRG_FLAG_OVERFLOW_SET) == _08_TRG_FLAG_OVERFLOW_SET)
         TRGSR0 &= (uint8_t)~_08_TRG_FLAG_OVERFLOW_SET;
         g_tmrg_overflow_count_a +=
         g_tmrg_overflow_count_b += 10L;
     if ((TRGSR0 & _02_TRG_FLAG_CAPTURE_COMPARE_B_SET) == _02_TRG_FLAG_CAPTURE_COMPARE_B_SET)
         TRGSR0 &= (uint8_t)~_02_TRG_FLAG_CAPTURE_COMPARE_B_SET;
         if (OUL == g_tmrg_overflow_count_b)
              temp = g_tmrg_old_value_b;
             g_tmrg_active_width_b = (uint32_t)(TRGGRB - temp);
         else
         ł
              temp = 0x10000UL * g_tmrg_overflow_count_b;
             g_tmrg_overflow_count_b =
             g_tmrg_overilow_count_b = 000;
temp = temp - g_tmrg_old_value_b;
g_tmrg_active_width_b = (uint32_t)(temp + TRGGRB);
         g_tmrg_inactive_width_b = OUL;
         g_tmrg_old_value_b = (uint32_t)TRGGRB;
        Start user code for r_TRG_input_interrupt. Do not edit comment generated here */
     /* End user code. Do not edit comment generated here */
```

Figure 3-4 Add the user code area



3.2.2 Improvement for Internal reference voltage can be used when VDD ≥ 2.4V in Comparator

When VDD \geq 2.4 V which includes 2.4 V \leq VDD \leq 5.5 V, 2.7 V \leq VDD \leq 5.5 V, 4.0 V \leq VDD \leq 5.5 V, Internal reference voltage can be selected as reference voltage.

VDD setting:	2.7 V ≤ VDD ≤ 5.5 V	
	4.0 V ≤ VDD ≤ 5.5 V	
High-speed on	2.7 V ≤ VDD ≤ 5.5 V	
Frequency:	2.4 V ≤ VDD ≤ 5.5 V	
Figu	re 3-5 VDD se	etting on [Clocks] page

Reference voltage setting Reference voltage V

Figure 3-6 Internal reference voltage can be selected

3.2.3 Improvement for Internal reference voltage can be used when VDD ≥ 2.4V in A/D converter

When VDD \ge 2.4 V which includes 2.4 V \le VDD \le 5.5 V, 2.7 V \le VDD \le 5.5 V, 4.0 V \le VDD \le 5.5 V, Internal reference voltage can be selected as A/D channel selection.

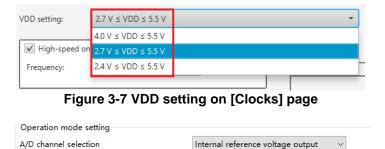


Figure 3-8 Internal reference voltage can be selected

Note: CTSU TSCAP voltage, Temperature sensor output voltage should have same spec as Internal reference voltage output in RL78/G16.

3.2.4 Improvement for adding PMC setting for INTP and TAU pins' setting

When using INTP5(P01), INTP7(P21), INTP7(P02) or TO00(P21) pin, the related PMC should be set 0. Smart Configurator adds related PMC setting code in API R_{Configuration Name}_Create().

3.2.5 Improvement for the specification according to RL78G16 UM from V0.9 to V1.0

Improved the specification according to RL78G16 User's Manual Hardware V1.0. Please refer to chapter "REVISION HISTORY" in User's Manual Hardware for detail.

3.2.6 Improvement for the specification according to RL78G24 UM from V0.8 to V1.0

Improved the specification according to RL78G24 User's Manual Hardware V1.0. Please refer to chapter "REVISION HISTORY" in User's Manual Hardware for detail.



3.2.7 Improvement for adding include path to build setting by default after code generation

From Smart Configurator for RL78 V1.7.0, Smart Configurator can add include path "\${workspace_loc:/\${ProjName}/src/smc_gen}" in default project e² studio. If the user changes the code generation path, Smart Configurator can add new include path and remove old include path into build setting by default after code generation.

Smart_Configrator_Example.scfg ×	- 8
Overview information	🔋 🤷 Generate Code 🛛 Generate Report
- General Information	•
Overview Get an overview of the features provided by Smart Configurator. Sector of the features provided by Smart Configurator. Wideos Introduction to Smart Configurator Browse related videos Sector of the features provided by Smart Configurator. What's New Check out what's new in the latest release. User manual and release notes Application Notes Tool news	Application Code Software Components Middleware & Drivers Device Drivers MCU Hardware
✓ Current Configuration	
Selected board/device: R7F100GSNxFB (ROM size: 768KB, RAM Generated location (PROJECT_LOC)) user_src\user_gen Selected components: Overview Board Clocks System Components Pins Interrupt	M size: 48KB, Pin count: 128) Edit

Figure 3-9 The user changes code generation path

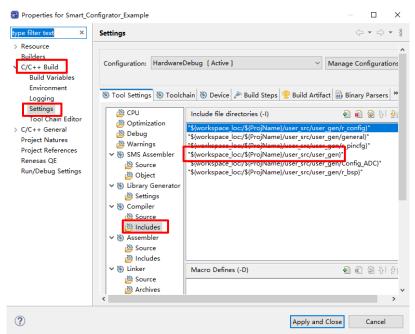


Figure 3-10 Add include path after code generation automatically



4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicabl e MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function https://www.renesas.com/document/tnn/notes- e-studio-smart-configurator-plug-smart- configurator-rI78	RL78/G23	V1.2.0
Mar. 16, 2022	R20TS0822	1. Notes when build or clean e ² studio Smart Configurator project <u>https://www.renesas.com/document/tnn/notes-</u> <u>e-studio-smart-configurator-plug-smart-</u> <u>configurator-rl78-0</u>	RL78/G23	V1.3.0
Dec. 01, 2022	R20TS0895	1. Notes when changing version of Board Support Program (BSP) or RL78 Software Integration System (SIS) modules <u>https://www.renesas.com/us/en/document/tnn/</u> <u>notes-e-studio-smart-configurator-rl78-plug-</u> <u>smart-configurator-rl78</u>	RL78/G23 RL78/F24 RL78/G15	V1.5.0



Smart Configurator for RL78 Plug-in in e² studio 2023-07

Smart Configurator for RL78 V1.7.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.7.0.

5.1 List of Limitation

Table 5-1 List of Limitation

Table 5-1 List of Limitation					: A	ppli	icat	ole,	-: Not Applicable
No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Note on extra help document issue	✓	✓	✓	✓	✓	>	✓	
	Note on ELCL D flip flop component GUI warning display incorrectly	1	-	-	-	-	-	-	
3	Note on the unsupported setting items for some ELCL components	<	-	I	1	1	-	1	
4	Note on the extra "Run" menu on toolbar	>	<	>	>	<	>	<	
5	Note on clock mode setting error in IICA	-	-	-	-	-	I	~	

5.2 **Details of Limitation**

Note on extra help document issue 5.2.1

For Smart Configurator, there is an extra help "Smart Browser" under "[Help] > [Help Contents]". Please ignore it.

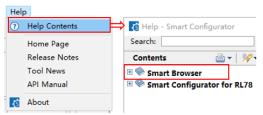


Figure 5-1 Extra help issue



5.2.2 Note on ELCL D flip flop component GUI warning display incorrectly

When selecting the event signal in ELCL D flip flop component, even if the selected signal consists with the hardware specification, there still displays the warning on the GUI.

[Avoidance measure]

Make reference to the hardware manual and set the selectable event signal though warning appeared in GUI, the waring is no impact for the code generation.

The following is example of using flip-flop 0 and flip-flop 1 in ELCL logic cell block L1.

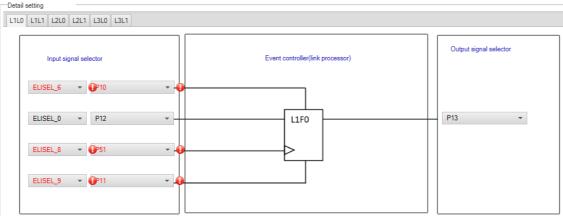


Figure 5-2 The flip-flop 0 in ELCL logic cell block L1 usage example

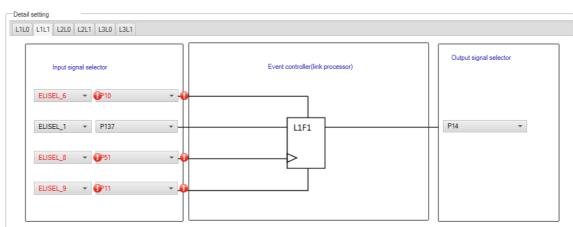


Figure 5-3 The flip-flop 1 in ELCL logic cell block L1 usage example



5.2.3 Note on the unsupported setting items for some ELCL components

In the following ELCL modules, it is not possible to set "no selection (fixed to 0)" as the input signal of the logic cell block and "negative logic output (inverted)" as the output level of the event signal.

- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

[Avoidance measure] None

5.2.4 Note on the extra "Run" menu on toolbar

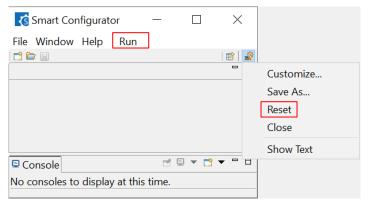
After launching Smart Configurator, an extra menu "Run" will appear on the toolbar if user has launched the Smart Configurator for RL78 V1.6.0 or earlier version. Please ignore this menu.

💰 Smart Configurat	or	_	
File Window Help	Run]	

Figure 5-4 Menu "Run" on the toolbar

To remove it, user can reset the perspective according to below steps:

1) Right-click Smart Configurator icon, select "Reset".





Smart Configurator for RL78 Plug-in in e² studio 2023-07 Smart Configurator for RL78 V1.7.0

2) Select "Reset Perspective".		
	🔇 Smart Configurator	- 🗆 X
	File Window Help	
	📬 🗁 🗐	
	C	
	Reset Perspective	×
	Reset the Smart Configurator perspective to its defaults?	
	Reset Perspective	No

Menu "Run" is removed.

ổ Smart Cor	nfigurator	—		\times
File Window	Help			
i 📬 🖿 🗐				i 🗈 📓
		- 0	🗖 M	×□□
Console ×		🚨 Config	urati	×
	E 🔻 🖻 🔻			7 8

5.2.5 Note on clock mode setting error in IICA

When user selects fCLK as 48MHz in [Clock] page, if user selects fCLK/2 as IICA operation clock, there are a "!" on GUI.

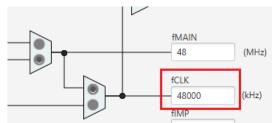


Figure 5-5 fCLK setting in [Clock] page

Clock mode setting		_	1
Clock mode setting	fCLK/2	- e	L

Figure 5-6 IICA operation clock error when selecting fCLK/2

[Avoidance measure]

The generation code is correct, so please ignore this error message.



6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.7.0.

6.1 List of Caution

Table 6-1 List of Caution

✓ : Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	1	1	-	1	1	-	1	
	Note on the installation of the Smart Configurator	1	✓	✓	1	✓	✓	✓	
	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	_	1	-	-	-	-	1	
4	Note on pulse width calculation of Timer RD input capture function	-	<	-	-	-	-	<	
	Note on using Touch middleware and UART communication components	1	-	-	-	-	-	-	
	Note on the include path update issue when renaming the component's configuration name	1	~	~	1	~	1	~	
	Note on TAU Input Signal High/Low level Measurement components.	1	~	~	1	~	1	~	
8	Note on C++ project of CC-RL V1.12	<	1	1	<	1	<	~	
	Note on browsing "Release Notes" and "Tool News" URL from the help menu	1	1	1	-	-	-	-	
10	Note on using user code protection feature	1	1	1	1	1	1	✓	
11	Note on IAR build error when using SMS function	✓	-	-	-	-	-	-	
	Note on A/D conversion time setting after performing [Change device] or [Change resource]	1	1	1	1	1	1	1	
13	Note on changing Hardware Debug Configuration on project generation wizard	1	1	1	1	1	1	1	
	Note on FAA Configurator component does not support LLVM project	_	-	-	-	-	-	1	



6.2 Details of Caution

6.2.1 Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"

When user use many components and DTC component together, the generated code build might fail due to some section address overlaps.

■ Console ×	🗶 ϟ 😚 🔄 🏭 🏭 = 🖳 🥃 🚽 💆 🕶 🗖 🕶 🗖
CDT Build Console [LLVM_R7F100GCJxLA_case1]	
<pre>ld.lld: error: section .bss virtual address range</pre>	overlaps with .dtc_vectortable
<pre>>>> .bss range is [0xF9F00, 0xF9F31]</pre>	
<pre>>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]</pre>	
ld.lld: error: section .bssf virtual address range	overlans with dtc controldata 0
<pre>>>> .bssf range is [0xF9F32, 0xF9F7F]</pre>	over taps with .ucc_concrotuata_o
>>> .dtc controldata 0 range is [0xF9F40, 0xF9F47]	
<pre>ld.lld: error: section .bss load address range ove</pre>	rlaps with .dtc_vectortable
<pre>>>> .bss range is [0xF9F00, 0xF9F31]</pre>	
<pre>>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]</pre>	
ld.lld: error: section .bssf load address range ov	erlaps with .dtc controldata 0
>>> .bssf range is [0xF9F32, 0xF9F7F]	
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]	
clang: error: ld.lld command failed with exit code	· · · · · · · · · · · · · · · · · · ·
makefile:110: recipe for target 'LLVM_R7F100GCJxLA	_case1.elf' failed
<pre>make: *** [LLVM_R7F100GCJxLA_case1.elf] Error 1 "make -j8 all" terminated with exit code 2. Build</pre>	might he incomplete
make - jo all terminated with exit code 2. Build	might be incompiete.
18:09:07 Build Failed. 2 errors, 0 warnings. (took	(15.846ms)
	· · · · · · · · · · · · · · · · · · ·

Figure 6-1 Build error message

[Workaround]

The Smart Configurator cannot set ".bss" and ".bssf" section address. So user should consider to modify ".bss" and ".bssf" section address manually in "linker_script.ld" file or change the DTC base address to avoid such section overlap error.

Configure	
Base setting	
DTC base address	0xF9F00

Figure 6-2 DTC base address setting



6.2.2 Note on the installation of the Smart Configurator

Do not set more than 64 characters for the installation directory.

You might see an error message "The specified path is too long" and will not be able to install Smart Configurator.

6.2.3 Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time

If user sets up TRDIOA0 for Input capture and TRDIOB0 for Output compare at the same time. Smart Configurator will output a Peripheral conflict error.

User can ignore this Smart Configurator error message and use these two functions at the same time.

6.2.4 Note on pulse width calculation of Timer RD input capture function

The pulse width calculation code is with the assumption that the counter is not cleared between two interrupts occurrence, except the input pulse width which is selected as counter clear trigger on GUI. For example, when "Clear by TRDGRAn input capture" is selected, only TRDIOAn pulse width calculation handle counter clear, other input pulse width calculation doesn't handle counter clear.

ter clear	Clear by TRDGRA0 input capture	
<pre>atic voidnear r_Config_TRD0_trd0_in uint16_t tmrd_pul_a_cur = TRDGRA0; uint16_t tmrd_pul_b_cur = TRDGRA0; uint16_t tmrd_pul_d_cur = TRDGRC0; uint16_t tmrd_pul_d_cur = TRDGRC0; uint16_t trdier0_temp = TRDIER0; TRDIER0 = 0x00U; /* overflow process */</pre>	<pre>terrupt(void) _FLAG) == _10_TRD_INTOV_GENERATE_FLAG)</pre>	
<pre>g_tmrd0_ovf_b += 10; g_tmrd0_ovf_c += 10; g_tmrd0_ovf_d += 10; } /* TRDGRA0 input capture interrupt *</pre>		
<pre>if ((TRDSR0 & _01_TRD_INTA_GENERATE_ { TRDSR0 &= (uint8_t) ~ 01_TRD_INTA, if (00 == g_tmrd0_ovf_a) { g_tmrd0_active_width_a = (ui } else { g_tmrd0_active_width_a = (ui } } }</pre>		cur);
g_tmrd0_ovf_a = 0U; }	The pulse width calculation handle counter clear.	
<pre>/* TRDGRB0_ipput_capture_ipterrupt_* if ((TRDSR0 & _02_TRD_INTB_GENERATE_</pre>		
<pre>{ TRDSR0 &= (uint8_t)~_02_TRD_INTB if (0U == g_tmrd0_ovf_b) / </pre>	_GENERATE_FLAG;	
<pre>g_tmrd0_active_width_b = (ui } else</pre>	<pre>nt32_t) ((uint32_t)tmrd_pul_b_cur - (uint32_t)g_tmrd0_trdgrb_old);</pre>	
	<pre>nt32_t)(((0x10000UL * (uint32_t)g_tmrd0_ovf_b) + (uint32_t)tmrd_pul_b - (uint32_t)g_tmrd0_trdgrb_old);</pre>	_cur)
<pre>g_tmrd0_inactive_width_b = 0UL;</pre>	lse width calculation doesn't handle counter clear	r

Figure 6-3 Counter clear setting in Input capture function



6.2.5 Note on using Touch middleware and UART communication components

When use Touch middleware, please do not change the name of UART components. Otherwise, due the file name mismatch will bring build error.

For example, in touch middleware select UART0 as UART channel, for UART0 component please use Config_UART0.

Components	Configure	0
type filter text	Property 🗸 🌼 Configurations	Value
V 🗁 Startup	# Parameter check	Use system default
V > Generic	# Support QE monitor using UART	Disable
♂ r_bsp	# Support QE tuning using UART	Disable
V > Drivers	# UART channel	UARTO
V Communications		
Config_UART0		
✓		
∽ 🗁 Generic		
💣 r_ctsu		

Figure 6-4 Touch middleware and UART communication components

6.2.6 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e² studio Smart Configurator project that has selfdefined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon

 $(\stackrel{lef}{\leftarrow})$ on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.

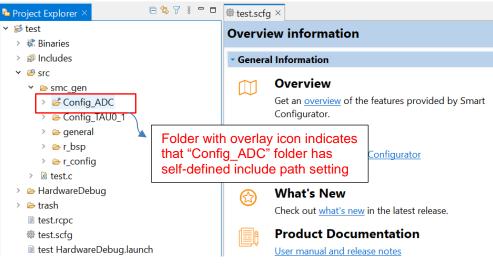


Figure 6-5 Interval Timer component configuration before renaming



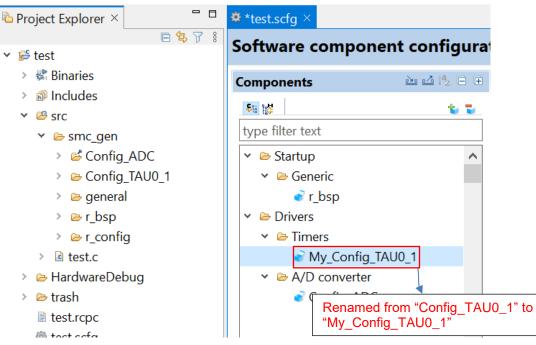


Figure 6-6 The Interval Timer component configuration after renaming

Properties for Cor	fig_ADC			_	
	Paths and Symbols				⇔ ▼ ⇔ ▼ ∦
 Resource C/C++ Build C/C++ General Paths and Sym Preprocessor I 	Configuration: Hardwa		· · ·	Manage C	onfigurations
Run/Debug Settir	 Includes # Symbol: Languages GNU C GNU C++ 	Include directorie	s	^	Add Edit
	Assembly Assembly	^I /\${ProjName}/ ^I /\${ProjName}/	/src/smc_gen/r_config /src/smc_gen/Config_ADC /src/smc_gen/general /src/smc_gen/Config_TAU0_1	~	Delete Export Move Up
	 "Preprocessor Incluid" ✓ Show built-in value ✓ Import Settings 		tc." property page may define additiona	l entries	Move Down
< >> ?		,	Include path for rename updated after code re-g To avoid build error, ple "Config_TAU0_1" to "M	jenerat ease m	tion. anually updat

Figure 6-7 Include path setting for the "Config_ADC" configuration



6.2.7 Note on TAU Input Signal High/Low level Measurement component

When using TAU Input Signal High/Low level Measurement component, after used noise filter function for TImn input pulse, please make sure the High/Low level width min value needs to be greater than two times the minimum value prompted on the UI.

For example, the High/Low level width min value is 0.032us (min value), when use noise filter function, the width min value should be 0.064us.

Clock setting		
Operation clock	CK00	~
Clock source	fCLK	~
(Clock frequency: 32000 kHz High-/low-leve	l width range: 0.032 (µs) ≤ TI00 ≤ 4.096 (ms))

Figure 6-8 High/Low level width min value

6.2.8 Note on CC-RL V1.12 C++ project

In CC-RL V1.12 C++ project, there are some dummy issues such as "EI()" in editor. However this is editor specification and does not affect the program operation. Please ignore it.

<pre> * DISCLAIMER[* File Name : Smart_Configurator_CPP_Example.cpp[#ifdef cplusplus </pre>
extern "C" {
#endif
<pre>#include "r_smc_entry.h"</pre>
<pre> #ifdefcplusplus </pre>
}
#endif
<pre>int main(void);</pre>
⊖ int main(void)
t
EI();
return 0;
}

Figure 6-9 CODAN issue in CC-RL V1.12 C++ project

6.2.9 Note on browsing "Release Notes" and "Tool News" URL from the help menu

For Smart Configurator for RL78 V1.4.0 or before version, "Release Notes" and "Tools News" in the help menu cannot access the correct URL. This issue has been fixed from this version. Please access the URL below directly for Smart Configurator for RL78 V1.4.0 or before version. Release Notes: <u>https://www.renesas.com/rl78-smart-configurator-release-note</u> Tool News: <u>https://www.renesas.com/rl78-smart-configurator-tn-notes</u>

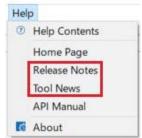


Figure 6-10 Release Notes and Tool News in Smart Configurators



6.2.10 Note on using user code protection feature

From Smart Configurator for RL78 V1.5.0 onwards, user code protection feature will be supported for all Code Generation components. Please use the following specific tags to add user code when using the user code protection feature. If the specific tags do not match exactly, inserted user code will not be protected after the code generation.

/* Start user code */

User code can be added between the specific tags

/* End user code */

The user code protection feature will only be supported on the files that are generated by the Code Generation component. Hence, the user code protection feature is not available for non-Code Generation components.

6.2.11 Note on IAR build error when using SMS component

When using SMS component, if the following build error is met in IAR Embedded workbench, please check the build order setting in project [Options...] -> [Custom Build] page.

- 1) When using IAR Embedded workbench V5.10, select "Run before compiling/assembling" (refer to Figure 6-12)
- 2) When using IAR Embedded workbench V4.21, make "Run this tool before all other tools" checked (refer to Figure 6-13)

The above setting can eliminate this build error.

Bui	ld		
	Messages	File	Line
8	Cleaning_1 files. r_bsp_common_jar.asm cstartup s Config_SMS c Fatal Enrol(Pe1696): cannot open source file "Config_SMS_ASM.h" searched: "C\cases\tempcase\typ_temp_case\g23\g23\g23\sr_20230321\srcksmc_gen\Config_SMS\t searched: "C\cases\tempcase\typ_temp_case\g23\g23\g23\sr_20230321\srcksmc_gen\genren\t searched: "C\cases\tempcase\typ_temp_case\g23\g23\g23\sr_20230321\srcksmc_gen\genren\t searched: "C\cases\tempcase\typ_temp_case\g23\g23\g23\sr_20230321\srcksmc_gen\genren\t searched: "C\cases\tempcase\typ_temp_case\g23\g23\g23\sr_20230321\srcksmc_gen\genry_config\t searched: "C\cases\tempcase\tempcase\typ_temp_case\g23\g23\g23\sr_20230321\srcksmc_gen\genry_config\t searched: "C\Program Files\AR Systems\Embedded Workbench 31\ty78\ind\t current directory: "C\cases\tempcase\typ_temp_case\g23\g23\gr_2023\srcksmc_gen\genry_config\t searched: "C\Program Files\AR Systems\Embedded Workbench 31\ty78\ind\t current directory: "C\cases\tempcase\typ_temp_case\g23\g23\g23\srcksmc_gen\genry_config\t searched: "C\Program Files\AR Systems\Embedded Workbench 31\ty78\ind	C\cases\tempcases\vcp_temp_case\g23\g23iar_20230321\src\smc_gen\Config_SMS\Config_SMS.c	38

Figure 6-11 IAR build error

Category:					
General Options					
Static Analysis					
C/C++ Compiler					
Assembler	Custom Tool Co	onfiguration			
Output Converter					
Custom Build	Filename exte	nsions:			
Build Actions	.smsasm				
Linker					
Debugger	Command line	9:			
COM Port E1	CADrogram	Files (x86)\Renesas Electronics\SMS\bin\smsasm.exe"	¢CI		
E1 F2	C:\Program Files (xoo)\Renesas Electronics\Sivis\bin\smsasm.exe				
E20	Output files (one per line):				
E2 Lite / E2 On-board	\$FILE BPATH	\$ h	~		
EZ-CUBE		****			
EZ-CUBE2					
Simulator			\vee		
тк			-		
	Additional inp	ut files (one per line):			
			\wedge		
			\vee		
			_		
	Build order:	Automatic (based on input and output)	\sim		
		Automatic (based on input and output)	_		
		Run before compiling/assembling			
		Kun before linking			

Figure 6-12 "Build order" setting of IAR Embedded workbench V5.10

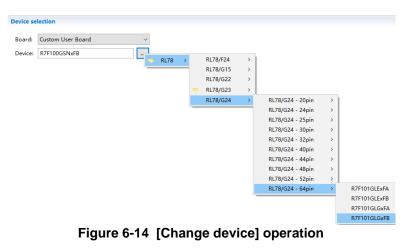


Category:	
General Options	
Static Analysis	
C/C++ Compiler	
Assembler	Custom Tool Configuration
Output Converter	
Custom Build	Filename extensions:
Build Actions	smsasm
Linker	
Debugger COM Port	Command line:
E1	"C:\Program Files (x86)\Renesas Electronics\SMS\bin\smsasm.exe" \$FI
E2	C.(riogram mes (xoo) (renesas Electromes (sivis (bin (sinsasin.exe - \$11
E20	Output files (one per line):
E2 Lite / E2 On-board	\$FILE_BPATH\$.h
EZ-CUBE	\$FILE_DPATH\$.0
EZ-CUBE2	
IECUBE	v .
Simulator	
тк	Additional input files (one per line):
	A
	v
	Run this tool before all other tools
	Kun this tool before all other tools
	0K Cancel
	UK Calicel

Figure 6-13 Custom build setting of IAR Embedded workbench V4.21

6.2.12 Note on A/D conversion time setting after performing [Change device] or [Change resource]

After performing [Change device] (for example, change from RL78/G23 to RL78/G24), the A/D conversion time setting can't be kept. The user should take note to reconfirm the conversion time setting as he wants.



Conversion time setting		
Conversion time mode	Normal 1	~
Conversion time	184/fCLK	~

Figure 6-15 A/D conversion time setting

When changing resource, for example from RL78/G24 normal A/D and RL78/G24 advanced A/D, the A/D conversion time can't be kept.

✓		Conversion time setting		
Communications	Generate code Output only initialization API Change resource	Please set fCLK not greater than 32MHz. Conversion time mode Normal 1		
		Conversion time	2112/fCLK	~

Figure 6-16 [Change resource] operation



6.2.13 Note on changing Hardware Debug Configuration on project generation wizard

When a target board (except custom) is selected during creating a new project, please don't change the Hardware Debug Configuration manually. The reason is that the Hardware Debug Configuration has be decided by target board automatically. The user setting can't be reflected into Smart Configurator.

Toolchain Sett	tings	
Language:		
Toolchain:	Renesas CC-RL \sim	
Toolchain Ver	sion: v1.12.00 ~	
	Manage Toolchains	
Device Setting	15	Configurations
Target Board:	RL78G23-128p_FastPrototypingBoard 🗸	Create Hardware Debug Configuratio
		COM Port (RL78)
Target Device	R7F100GSNxFB	Create Debug Configuration
	Unlock Devices	RL78 Simulator
Endian	: Little 🗸	RL/8 Simulator
Project Type:	: Default 🗸	Create Release Configuration

Figure 6-17 Select a target board when creating a project in e² studio

6.2.14 Note on FAA Configurator component does not support LLVM project

In Smart Configurator for RL78 V1.7.0, FAA Configurator component was not supported for LLVM project. Though the user can add FAA Configurator component under LLVM project, but the generated FAA source code can't be built successfully and works for running and debugging.



Smart Configurator for RL78 Plug-in in e² studio 2023-07

Smart Configurator for RL78 V1.7.0

Revision History

Rev.	Section	Description
1.00	-	First edition issued



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied to the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pullup power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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