

RENESAS TECHNICAL UPDATE

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|--------------------|--|---------|----------------------|--|------|------|
| Product Category | MPU/MCU | | Document No. | TN-RA*-A0108A/E | Rev. | 1.00 |
| Title | Addition of note for Slave Bus Control Register in Buses chapter | | Information Category | Technical Notification | | |
| Applicable Product | RA4E1 Group RA4M2 Group | Lot No. | Reference Document | Renesas RA4E1 Group User's Manual: Hardware Rev.1.10 Renesas RA4M2 Group User's Manual: Hardware Rev.1.30 | | |
| | | All | | | | |

Note for Slave Bus Control Register in Buses chapter is added.

14.3.3 BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU, EQBIU)

Note: While both of the following two conditions are met, the CPU may occupy the bus and DMAC/DTC data transfer may not be prioritized.

- Condition 1
DMAC/DTC accesses FHBIU, FLBIU, S0BIU, EQBIU, and CPU fetches instructions from the same BUS slaves.
- Condition 2
CPU instruction fetch loops through a specific address. For example, waiting time by software.
Example: loop1:subs r0,#1
 cmp r0,#0
 bne loop1

To avoid this problem, set DMAC/DTC access bus and CPU instruction fetch to different BUS Slaves.

Example: DMAC/DTC accesses S0BIU (SRAM0 or Standby RAM), and CPU fetches instructions from FHBIU.

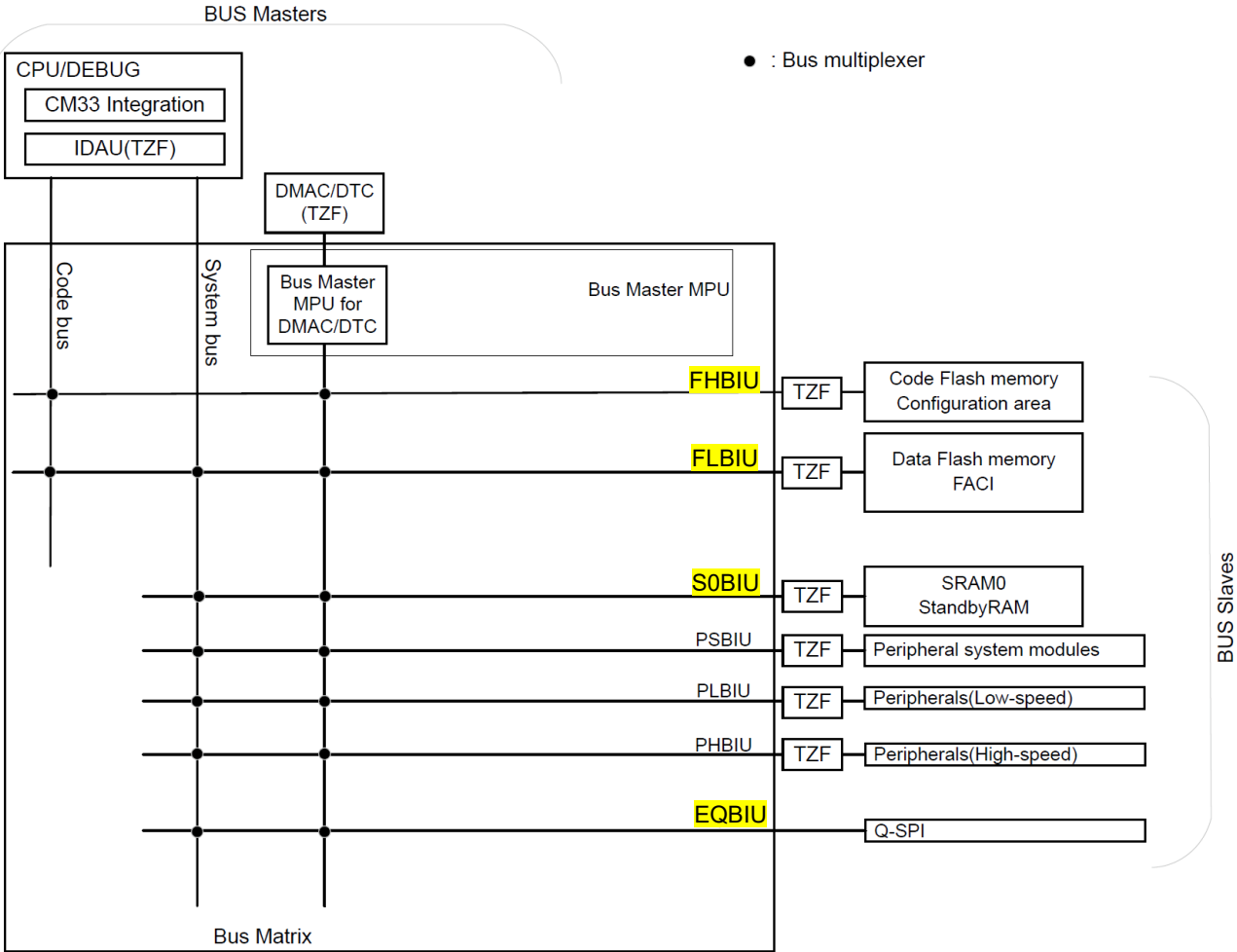


Figure 14.1 Bus Connection

| | |
|-------------|---|
| 0xFFFF_FFFF | System for Cortex®-M33 |
| 0xE000_0000 | Reserved area*2 |
| 0x6800_0000 | External address space (Quad SPI area) |
| 0x6000_0000 | Reserved area*2 |
| 0x4080_0000 | Flash I/O registers |
| 0x407F_C000 | Reserved area*2 |
| 0x407F_0000 | Flash I/O registers |
| 0x407E_0000 | Reserved area*2 |
| 0x4018_0000 | Peripheral I/O registers |
| 0x4000_0000 | Reserved area*2 |
| 0x2800_0400 | Standby SRAM |
| 0x2800_0000 | Reserved area*2 |
| 0x2002_0000 | SRAM0 |
| 0x2000_0000 | Reserved area*2 |
| 0x0800_2000 | On-chip flash (data flash) |
| 0x0800_0000 | Reserved area*2 |
| 0x0100_A300 | On-chip flash (option-setting memory) |
| 0x0100_A100 | Reserved area*2 |
| 0x0100_81B4 | On-chip flash (Factory Flash) |
| 0x0100_80F0 | Reserved area*2 |
| 0x0008_0000 | On-chip flash (code flash) (read only)*1 |
| 0x0000_0000 | |

Figure 4.1 Memory map