To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A405A/E	Rev.	1.00
Title	Correction of errors in the H8SX/1653 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1653 Group	Lot No. All lots	Reference Document	H8SX/1653 Group Hardware Manual (REJ09B0219-0100)		

We would like to inform you of the correction of errors in the above hardware manuals. Please refer to the following for details.

<Corrections>

Section 5 Interrupt Controller

Deletion of DTCERF, DTCERG, and DTCERH
(1) Page 117, 5.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

- Description omitted (no changes) –

[After Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to **DTCERE** of the DTC.

- Description omitted (no changes) –

(2) Page 118, 5.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(3) Operation Order

- Description omitted (no changes) –

Table 5.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERH of the DTC, and the DISEL bit in MRB of the DTC.

[After Change]

(3) Operation Order

- Description omitted (no changes) –

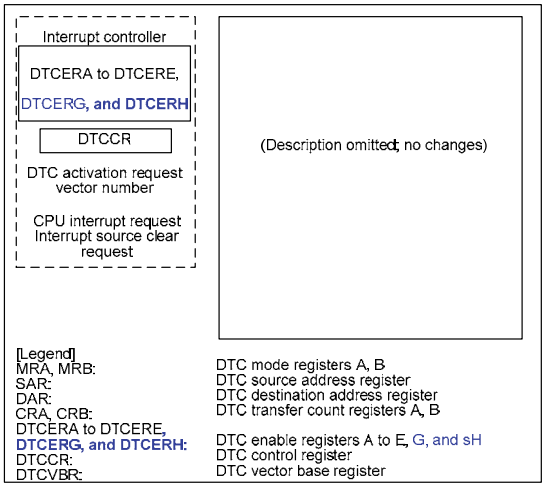
Table 5.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to **DTCERE** of the DTC, and the DISEL bit in MRB of the DTC.

Section 8 Data Transfer Controller

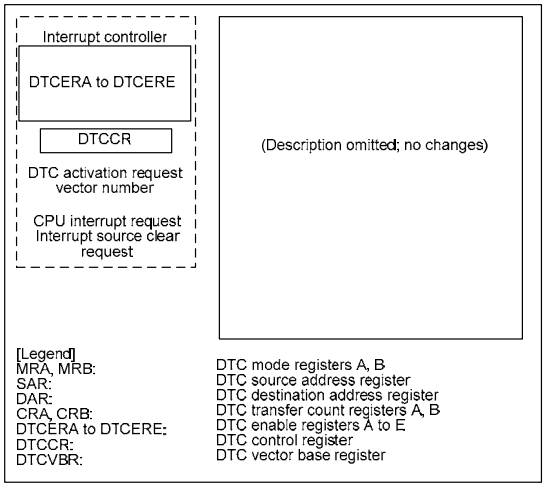
Deletion of DTCERG, and DTCERH in DTCER

(1) Page 308, DTCER description in figure 8.1, Block Diagram of DTC

[Before Change]



[After Change]



(2) Page 309, section 8.2, Register Descriptions

Deletion of DTCERG, and DTCERH in DTCER

[Before Change]

- DTC enable registers A to E**, G, and H** (DTCERA to DTCERE, **DTCERG, and DTCERH**)

[After Change]

- DTC enable registers A to E (DTCERA to DTCERE)

(3) Page 314, section 8.2.7, DTC Enable Register
Deletion of DTCERG, and DTCERH in DTCER
[Before Change]

8.2.7 DTC enable registers A to E**, G, and H** (DTCERA to DTCERE, **DTCERG, and DTCERH**)

DTCER, which is comprised of eight registers, DTCERA to DTCERE, **DTCERG, and DTCERH,** is a register that specifies DTC activation interrupt sources.

[After Change]

8.2.7 DTC Enable Register A to E (DTCERA to DTCERE)

DTCER, which is comprised of **five** registers, DTCERA to DTCERE, is a register that specifies DTC activation interrupt sources.

Section 9 I/O Ports

(1) Page 380, table 9.5, Available Output Signald and Settings in Each Port

[Before Change]

Port	Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$	SYSCRE.EXPE = 1, BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$)_OE	RD/$\overline{\text{WR}}$	SYSCR.EXPE = 1, PFCR2.REWRE = 1 or SRAMCR.BCSELn = 1

[After Change]

Port	Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$	SYSCRE.EXPE = 1, BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$)_OE	RD/$\overline{\text{WR}}$	SYSCR.EXPE = 1, PFCR2.**RDWRE** = 1 or SRAMCR.BCSELn = 1

Section 12 8-Bit Timers (TMR)

(1) Description in section 12.7.2, A/D Converter Activation on page 525.

[Before Change]

The A/D converter can be activated only by TMR_0 compare match A. *

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 by the occurrence of TMR_0 compare match A, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

Note: * Available only in unit 0 and unit 1.

[After Change]

The A/D converter can be activated only by **TMR_0 or TMR_2 compare match A**. *

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 **by the occurrence of compare match A,** a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

Note: * Available only in unit 0 and unit 1.

Section 14 Serial Communication Interface (SCI, IrDA, CRC)

(1) Page 561, the name of bit 4 in Serial Status Register (SSR)

[Before Change]

Serial Status Register (SSR)

- When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit Name	TDRE	RDRF	ORER	FRE	PER	TEND	MPB	MPBT
Initial Value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

[After Change]

- When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit Name	TDRE	RDRF	ORER	**FER**	PER	TEND	MPB	MPBT
Initial Value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

(2) Page 569, table 14.3, Relationships between N Setting in BRR and Bit Rate B

[Before Change]

Table 14.3, Relationships between N Setting in BRR and Bit Rate B

Mode	ABCS Bit	Bit Rate	Error
Asynchronous mode	0	$B = \frac{P\phi \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	Description omitted (no changes)
	1	$B = \frac{P\phi \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	

[After Change]

Table 14.3, Relationships between N Setting in BRR and Bit Rate B

Mode	ABCS Bit	Bit Rate	Error
Asynchronous mode	0	$N = \frac{P\phi \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	Description omitted (no changes)
	1	$N = \frac{P\phi \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	

Section 23 List of Registers

(1) Page 885, section 23.1 Register Addresses (Address Order)

Deletion of DTCERG and DTCERH in DTCER

[Before Change]

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access Cycles (Read/Write)
– Description omitted (no changes) –						
DTC enable register E	DTCERE	16	H'FFF28	INTC	16	2Iφ/3Iφ
DTC enable register G	**DTCERG**	**16**	**H'FFF2C**	**INTC**	**16**	**2Iφ/3Iφ**
DTC enable register H	**DTCERH**	**16**	**H'FFF2E**	**INTC**	**16**	**2Iφ/3Iφ**
DTC control register	DTCCR	8	H'FFF30	INTC	16	2Iφ/3Iφ
– Description omitted (no changes) –						

[After Change]

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access Cycles (Read/Write)
– Description omitted (no changes) –						
DTC enable register E	DTCERE	16	H'FFF28	INTC	16	2Iφ/3Iφ
DTC control register	DTCCR	8	H'FFF30	INTC	16	2Iφ/3Iφ
– Description omitted (no changes) –						

(2) Page 899, section 23.2, Register Bits

Deletion of DTCERG, and DTCERH in INTC

[Before Change]

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
– Description omitted (no changes) –									TPU_5
DTCERA to DTCERD	– Description omitted (no changes) –								INTC
DTCERE	–	–	DTCEE13	DTCEE12	–	–	–	–	
	–	–	–	–	–	–	–	–	
DTCERG	**–**	**–**	**–**	**–**	**DTCEG11**	**DTCEG10**	**–**	**–**	
	DTCEG7	**DTCEG6**	**–**	**–**	**–**	**–**	**–**	**–**	
DTCERH	**DTCEH15**	**DTCEH14**	**–**	**–**	**–**	**–**	**–**	**–**	
	–	**–**	**–**	**–**	**–**	**–**	**–**	**–**	
DTCCR	–	–	–	RRS	RCHNE	–	–	ERR	
INTCR to ISR	– Description omitted (no changes) –								
– Description omitted (no changes) –									I/O port

[After Change]

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
– Description omitted (no changes) –									TPU_5
DTCERA to DTCERD	– Description omitted (no changes) –								INTC
DTCERE	–	–	DTCEE13	DTCEE12	–	–	–	–	
	–	–	–	–	–	–	–	–	
DTCCR	–	–	–	RRS	RCHNE	–	–	ERR	
INTCR to ISR	– Description omitted (no changes) –								
– Description omitted (no changes) –									I/O port

(3) Page 912, section 23.3, Register States in Each Operating Mode

Deletion of DTCERG and DTCERH in INTC

[Before Chenage]

Register Abbreviation	Reset	Sleep	Module Stop	All-Module-Clock-Stop	Software Standby	Hardware Standby	Module
			– Description omitted (no changes) –				TPU_5
DTCERA to DTCERD			– Description omitted (no changes) –				INTC
DTCERE	Initialized	–	–	–	–	Initialized	
DTCERG	**Initialized**	**–**	**–**	**–**	**–**	**Initialized**	
DTCERH	**Initialized**	**–**	**–**	**–**	**–**	**Initialized**	
DTCCR	Initialized	–	–	–	–	Initialized	
INTCR to ISR			– Description omitted (no changes) –				
			– Description omitted (no changes) –				I/O port

[After Change]

Register Abbreviation	Reset	Sleep	Module Stop	All-Module-Clock-Stop	Software Standby	Hardware Standby	Module
			– Description omitted (no changes) –				TPU_5
DTCERA to DTCERD			– Description omitted (no changes) –				INTC
DTCERE	Initialized	–	–	–	–	Initialized	
DTCCR	Initialized	–	–	–	–	Initialized	
INTCR to ISR			– Description omitted (no changes) –				
			– Description omitted (no changes) –				I/O port