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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RH8-B0111D/E	Rev.	4.00
Title	Errata of RH850/E1x User's Manual Hardware Rev.1.20		Information Category	Technical Notification		
Applicable Product	RH850/E1x-FCC1 RH850/E1M-S RH850/E1L	Lot No. -	Reference Document	Refer to the below		

1. Explanation

This document is errata of “RH850/E1x User's Manual Hardware Rev.1.20”.

No.1 to No.101 have already been notified on the previous edition of TN-RH8-B111C/E.

No.102 to No.107 are additional items.

[Reference Documents]

Series	Group	Title	Rev.	Document No.
RH850	E1x-FCC1	RH850/E1x-FCC1 User’s Manual: Hardware	1.20	R01UH0416EJ0110
RH850	E1M-S	RH850/E1M-S User’s Manual: Hardware	1.20	R01UH0466EJ0110
RH850	E1L	RH850/E1L User’s Manual: Hardware	1.20	R01UH0468EJ0110

Errata of RH850/E1x User's Manual Hardware Rev.1.20

The changes are shown below. (Error: red, Correct: blue)

PDF page (Rev.x.xxE) lists representative product E1x-FCC1. For details, refer to "UM (page) that applies the same correction" column.

No.	PDF Page (Rev.x.xxE)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note	UM (page) that applies the same correction		
									E1x-FCC1	E1M-S	E1L
1	ALL	ALL	–	–	Modified the multiple bits notation in bit chart to match the register contents' table.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		ALL	ALL	ALL
2	113	Pins	2.1.4.6 Pin-Unit Register (1) PCRn_m – Port Control Register	...access to them via the PCRn_m register does not require a protection unlock sequence. CAUTIONS ---------- · Multiple bits in the PCRn_m register can be batch-set within the ranges described in Section 2.1.4.7, Example of Port Configuration Flow (2), Individual Setting. · If the bits are batch-set out of the range for setting of PCRn_m, the pin may output an unexpected signal level. ----------	...access to them via the PCRn_m register does not require a protection unlock sequence. CAUTIONS ---------- · Multiple bits in the PCRn_m register can be batch-set within the ranges described in Section 2.1.4.7, Example of Port Configuration Flow (2), Individual Setting. · When PMn_m = 1 and PMCn_m = 1, input is enabled. Configure the PUn_m/PDn_m setting in advance to prevent shoot-through current when pins are open or mid-range potential is input to them. · If the bits are batch-set out of the range for setting of PCRn_m, the pin may output an unexpected signal level. ----------	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		113	99	98
3	241	CPU System	(1) ICTAGL – Instruction cache tag Lo access register	Bit Position | Bit Name | Function | R/W | Value after Reset 9 to 6 | – | Reserved for future expansion. When writing, always write 0 to these bits. | R | 0	Bit Position | Bit Name | Function | R/W | Value after Reset 9 to 7 | – | Reserved for future expansion. When writing, always write 0 to these bits. | R | 0 6 | – | Reserved for future expansion. When writing, always write 0 to these bits. | R | Undefined	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		241	203	196
4	244	CPU System	(7) ICERR – Instruction cache error register	Bit Position | Bit Name | | | Value After Reset 31 | CISTW | | | 0	Bit Position | Bit Name | | | Value After Reset 31 | CISTW | | | Undefined	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		244	206	199
5	258	CPU System	Table 3.67 Register Contents of IPGECRUM Function of VD	This bit is set to 1 when a violation of peripheral device protection is detected by a program with the relevant right. Even if another violation of peripheral device protection is detected while this bit is 1, data of this IPGECR register and the IPGADR register is not updated and is retained.	This bit is set to 1 when a violation of peripheral device protection is detected by a program with the relevant right. If another violation of peripheral device protection is detected, data of this IPGECRUM register and the IPGADRUM register is updated.	Description Change	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E" and "TN-HR8-B095A/E".		258	220	213
6	272	CPU System	Table 3.80 Features of the RH850G3K Core	N/A	Use the HALT instruction to stop the PCU when PCU is not used.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		272	234	227
7	277	CPU System	(b) EIPSW – Status save register when acknowledging EI level exception register @PCU	bit-map 0 : V	bit-map 0 : Z	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		277	239	232
8	279	CPU System	(d) FEPSW – Status save register when acknowledging FE level exception register @PCU	bit-map 0 : V	bit-map 0 : Z	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		279	241	234
9	280	CPU System	(e) PSW – Program status word register @PCU	bit-map 0 : V	bit-map 0 : Z	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		280	242	235
10	289	CPU System	(t) PID – Processor ID register @PCU Table 3.105 PID Register Contents Function identifier	Bit 23 to 11 : Reserved Bit 10 : Double-precision floating-point operation function Bit 9 : Single-precision floating-point operation function Bit 8 : Memory protection unit (MPU) function	Bit 23 to 9 : Reserved Bit 8: Memory protection unit (MPU) function	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		289	251	244
11	292	CPU System	(a) ISPR – Priority of interrupt being serviced register @PCU	bit-map 15,13,11,9 : N/A	bit-map 15,13,11,9 : 0	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		292	254	247
12	298	CPU System	(d) MPBRGN – MPU base region register @PCU	bit chart 4→0 : MPBRGN Table 3.118 MPBRGN Register Contents Bit Position : 31 to 5 – 4 to 0 MPBRGN	bit chart 3→0 : MPBRGN Table 3.118 MPBRGN Register Contents Bit Position : 31 to 4 – 3 to 0 MPBRGN	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	**Since there is an error in the section title, No.12 is fixed at No. 52.**	298	260	253
13	298	CPU System	(e) MPTRGN – MPU end region register @PCU	bit-map 4→0 : MPTRGN Table 3.119 MPTRGN Register Contents Bit Position : 31 to 5 – 4 to 0 MPTRGN	bit-map 3→0 : MPTRGN Table 3.119 MPTRGN Register Contents Bit Position : 31 to 4 – 3 to 0 MPTRGN	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	**Since there is an error in the section title, No.13 is fixed at No. 53.**	298	260	253
14	313	Address Space	Table 4.1 Address Space	(0001 7000H to 0001 7FFFH) | (FCU firmware area (Map is switched by FCUFAREA register))*3	(0001 7000H to 0001 7FFFH) | (FCU firmware storage area (Map is switched by FCUFAREA register))*3	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		313	275	268
15	335	Interrupt	6.2.11 TIMER – Timer Interrupt Mask Enable Register	When subblock 6 of the timer D is used only as an A/D converter or a trigger output to the DFE, set the IMEO bit to 1.	When subblock 4 of the timer D is used only as a DMA trigger source, set the IME2 bit to 1. When subblock 6 of the timer D is used only as an A/D converter or a trigger output to the DFE, set the IMEO bit to 1.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		335	297	–
16	414	DMA	7.9.2.7 DTSER2 – DTS Error Register 2	Name of Bit31 in bit chart RMADED	RAMDED	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		414	376	368
17	485	Power Supply Voltage Monitor	Table 10.1 Register Specifications	Register Name | … | Access Size CVM detection flag register | … | 32 CVM detection flag clear register | … | 32 CVM control register | … | 32 Upper limit voltage setting register | … | 32 Lower limit voltage setting register | … | 32 Detection signal filter control register | … | 32	Register Name | … | Access Size | Access Protection CVM detection flag register | … | 32 | CVM detection flag clear register | … | 32 | CVM control register | … | 32 | PROTOPHCMD Upper limit voltage setting register | … | 32 | Lower limit voltage setting register | … | 32 | Detection signal filter control register | … | 32 |	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		485	446	438
18	495	Clock Controller	11.1 Features	· The clock frequencies can be increased stepwise by software for suppressing inrush currents after release from the reset state. The division ratios for the CPU clock and the peripheral clocks can be selected with register settings (1/4, 1/2, and 1/1).	· The clock frequencies can be increased stepwise by software for suppressing inrush currents after release from the reset state. Set the division ratios (1/4, 1/2, and 1/1) for the CPU clock and the peripheral clocks, and follow the clock gear up sequence. *1 Note 1. In this product, set the division ratio of the divider OA/1A to 1/1 (No division) after executing the clock gear up sequence.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		495	456	448
19	496	Clock Controller	Table 11.1 List of Clocks	Clock Frequency Note3 N/A	Clock Frequency *3 Note 3. In this product, set the division ratio of the divider OA/1A to 1/1 (No division) after executing the clock gear up sequence.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		496	457	449
20	512	Clock Controller	11.5.1 Operation When the Divide Function Is Used	Follow the procedure given below to reduce current fluctuations produced by switching the clock signals during startup (also see Figure 11.3, Example of Sequence for Shifting the Clock Gear Up).	Follow the procedure given below to reduce current fluctuations produced by switching the clock signals during startup.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		512	473	465
21	517	Clock Controller	Table 11.16 Pin Specifications	Access Protection N/A Register Name | ~ | AccessSize Clock control register | ~ | 8 CKC flag register | ~ | 8 Clock select register | ~ | 8 BRGA0 compare register | ~ | 8 CKC protect command register | ~ | 8 CKC protect status register | ~ | 8	Register Name | ~ | AccessSize | Access Protection Clock control register | ~ | 8 | ACKOCKCPCMD CKC flag register | ~ | 8 | Clock select register | ~ | 8 | BRGA0 compare register | ~ | 8 | CKC protect command register | ~ | 8 | CKC protect status register | ~ | 8 |	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		517	478	470
22	693	RLIN2	15.3.3.15 RLN21nmLiDBRb – LIN Data Buffer b Register	· For response reception: The RLN21nmLiDBRm registers hold the data received in the response field. The received data is overwritten. If an error is detected, the data prior to reception interruption is stored in the register. Do not read these registers when the FTS bit is 1 (frame transmission or wake-up transmission/reception is started)	· For response reception: The RLN21nmLiDBRm registers hold the data received in the response field. The received data is overwritten. If an error is detected, the data up to the byte in which the error was detected are stored in the register. Do not read these registers when the FTS bit is 1 (frame transmission or wake-up transmission/reception is started)	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		693	654	645

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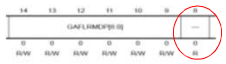
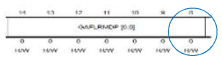
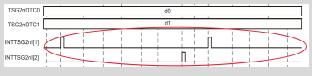
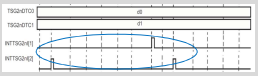
No.	PDF Page (Rev.x.xxE)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note	UM (page) that applies the same correction: E1x-FCC1	E1M-S	E1L
23	708	RLIN2	15.13 Status Table 15.35 shows the types of statuses available.	Status: Header reception end Status Set Condition: When a header field is transmitted successfully.	Status: Header transmission end Status Set Condition: When a header field is transmitted successfully.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		708	669	660
24	777	RS-CAN	16.3.2.15 RSCANDGAFLPOj – Receive Rule Pointer 0 Register (j = 0 to 15)			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		777	738	729
25	818	RS-CAN	16.3.2.42 RSCANOCFTISTS – Transmit/Receive FIFO Buffer Transmission Interrupt Flag Status Register	Bit chart Bit position 1 CHITXIF1	Bit chart Bit position 1 CFITXIF	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		818	779	770
26	935	FlexRay	17.2.4.3 FLXAOFREILS – FlexRay Error Interrupt Line Select Register	Name of Bit9 in bit chart IBAL	I IBAL	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		935	896	–
27	1085	FlexRay	17.2.13.2 FLXAOFROTS – FlexRay Output Transfer Status Register	Name of Bit11, 10 in bit chart Bit11 FWS Bit10 OWS	Bit11 FWIS Bit10 OWIS	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1085	1049	–
28	1232	RHSB	18.2.6.2 RHSBjIS – Interrupt Status Register	Name of Bit25 in bit chart RHSBjUE	RHSBjUEF	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1232	1193	902
29	1404	ATU-IV	21.4.2.8 TIOR2A – Timer I/O Control Register 2A (1) NCKGA0 to 6 – Noise Canceler Clock Select G A0 to 6	These bits select the count source clock of noise canceler counters A0 to 6 (NCNTGA0 to 6).	These bits select the count source clock of noise canceler counters A0 to 6 (NCNTA0 to 6).	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	**Since the correction information of E1L is missing, No.29 is modified to No.61.**	1404	1365	1065
30	1412	ATU-IV	Table 21.23 TILRA Register Contents	Bit Position | Bit Name 6 to 0 | TIALx	Bit Position | Bit Name 6 to 0 | TIAL0x	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1412	1373	1073
31		ATU-IV	Only Japanese UM is modified.			–	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".				
32	1559	ATU-IV	Table 21.92 TSRDx Register Contents	Bit Position | Bit Name 3 to 0 | CMFBDx2 to CMFBDx0	Bit Position | Bit Name 3 to 0 | CMFBDx3 to CMFBDx0	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1559	1520	1220
33	1632	ATU-IV	Table 21.117 TCR2Fx Register Contents	Bit Position | Bit Name 7 to 5 | EISELEFx	Bit Position | Bit Name 7 | EISELEFx	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1632	1593	1293
34		ATU-IV	Only Japanese UM is modified.			–	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".				
35	1951	TSG2	Figure 23.15 Interrupt Generation Example (1/2) (Example of HT-PWM Mode)			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	**Since the correction information is missing, No.35 is modified to No.62.**	1951	1912	1611
36	2062	TAPA	24.2.1 Registers Overview	Register Name | Function | R/W TAPAnACTS | TAPAn asynchronous control start trigger register | W TAPAnACTT | TAPAn asynchronous control stop trigger register | W TAPAnOPHS | TAPAn Hi-Z start trigger register | W TAPAnOPHT | TAPAn Hi-Z stop trigger register | W	Register Name | Function | R/W TAPAnACTS | TAPAn asynchronous control start trigger register | R/W TAPAnACTT | TAPAn asynchronous control stop trigger register | R/W TAPAnOPHS | TAPAn Hi-Z start trigger register | R/W TAPAnOPHT | TAPAn Hi-Z stop trigger register | R/W	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2062	2023	1722
37	2098	PIC	Table 25.19 PIC2DSADTEN1n0 Register Contents (About E1L, Table No. is 25.18.)	Bit Position | Bit Name 15 | PIC2DSADTEN1n115 14 | PIC2DSADTEN1n114 13 | PIC2DSADTEN1n113 12 | PIC2DSADTEN1n112 11 | PIC2DSADTEN1n111 10 | PIC2DSADTEN1n110 9 | PIC2DSADTEN1n109 8 | PIC2DSADTEN1n108	Bit Position | Bit Name 15 | PIC2DSADTEN1n015 14 | PIC2DSADTEN1n014 13 | PIC2DSADTEN1n013 12 | PIC2DSADTEN1n012 11 | PIC2DSADTEN1n011 10 | PIC2DSADTEN1n010 9 | PIC2DSADTEN1n09 8 | PIC2DSADTEN1n08	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2098	2059	1754
38	2184	ADCB	Table 26.45 Register Address List	Note: m = 0, 1: n = 0 to 39 About E1L: m = 0 : n = 0 to 35; m = 1 : n = 0 to 31	Note: m = 0, 1: n = 00 to 39 About E1L: m = 0 : n = 00 to 35; m = 1 : n = 00 to 31	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2184	2145	1838
39	2185	ADCB	26.10.4.1 FDRmn – Floating-Point Data Register mn	Note m = 0, 1: n = 0 to 39 About E1L: m = 0 : n = 0 to 35; m = 1 : n = 0 to 31	Note m = 0, 1: n = 00 to 39 About E1L: m = 0 : n = 00 to 35; m = 1 : n = 00 to 31	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2185	2146	1839
40		Safety	Only Japanese UM is modified.			–	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".				
41	2342	Safety	Table 29.32 LRTDATBFn_PE1 Register Contents	Bit Position | Bit Name 24 to 16 | LRTDATBF 8 to 0 | LRTDATBF	Bit Position | Bit Name 24 to 16 | LRTDATBF (2n+1) 8 to 0 | LRTDATBF (2n)	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2342	2303	1996
42	2497	ECM	30.3.4 ECMmESSTR0 (m = M/C) – ECM Master/Checker Error Source Status Register 0	Bit Name of Bit13 in bit chart ECMmSSE016	ECMmSSE013	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2497	2458	2150
43	2511	ECM	Table 30.24 ECMPCMD1 Register Contents	Bit Position | Bit Name 31 to 18 | –	Bit Position | Bit Name 31 to 8 | –	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2511	2472	2164
44	E1L only (UM P2204)	Flash Memory	Table 33.13 List of Registers Related to Product Information	Value after Reset See Section 33.9.3.1 (3 places)	Value after Reset See Table 33.14	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	2204
45	2567	Flash Memory	33.9.3.1 PRDNAMEn: n = 1 to 4 – Product Name Storage Register Table 33.15 List of Registers Related to Product Information	Bit Name PRDNAME[31:0]	PRDNAMEn[31:0]	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2567	2528	2205
46	E1L only (UM P2262)	Electrical Characteristics	37.3.6 CSIH Timing Note :	● n = 0 to 2, x = 0 to 5 (n = 0), x = 0 to 3 (n = 1, 2, 3)	● n = 0 to 2, x = 0 to 5 (n = 0), x = 0 to 3 (n = 1, 2)	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	2262
47	2645	Electrical Characteristics	Table 37.37 ADC Converter Characteristics (Depending on the product, table number is different.)	A/D conversion time (fOP = 20 MHz, 40 MHz)	A/D conversion time	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2645	2604	2277
48	2853, etc	Appendix Package Dimensions	Appendix Package Dimensions	Refer to "Package Dimensions(BGA)" sheet.	Refer to "Package Dimensions(BGA)" sheet.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2853, 2854	2812, 2813	2451

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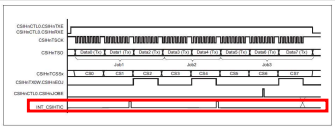
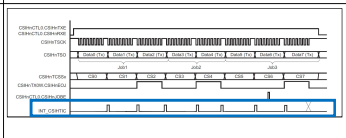
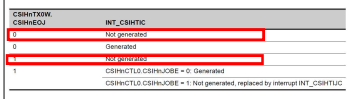
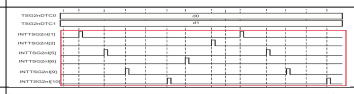
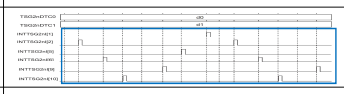
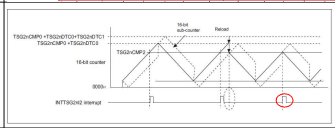
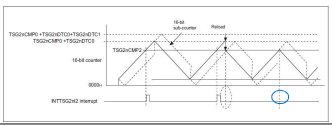
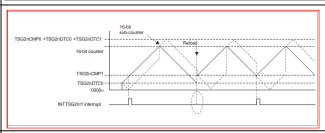
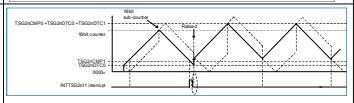
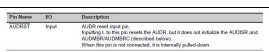
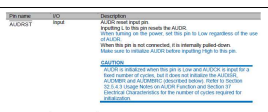
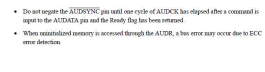
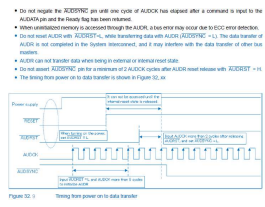
									E1x-FCC1	E1M-S	E1L
49	E1L only (UM P50)	Overview	1.2 Features Motor control timer (TSG2) Timer option (TAPA)	TSG2, TAPA: Two units are incorporated individually. ・Incorporates a timer unit that can control up to two 3-phase motor controls (U, V, and W).	TSG2, TAPA: One unit is incorporated individually. ・Incorporates a timer unit that can control up to one 3-phase motor control (U, V, and W).	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	50
50	265	CPU System	Table 3.76 SEGCONT Register Contents (1/2) bit 8	VCRE Notification of the detection of illegal access by the IPG and subsequent access blocking.*2	VCRE Notification of the detection of illegal access by the IPG and subsequent access blocking (including instruction fetch).*2	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		265	227	220
51	266	CPU System	Table 3.76 SEGCONT Register Contents (2/2) bit 4	VCIE ・Notification of a response to an error in the P-Bus (excluding errors in writing to the P-Bus). … ・Notification of a response to an error in the code flash	VCIE ・Notification of a response to an error in the P-Bus (excluding errors in writing to the P-Bus). … ・Notification of access detection to an unimplemented area in the on-chip I/O register (self) ・Notification of a response to an error in the code flash	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		266	228	221
52	298	CPU System	(3) MPBRGN – MPU base region register @PCU	bit chart 4→0 : MPBRGN Table 3.118 MPBRGN Register Contents Bit Position : 31 to 5 – 4 to 0 MPBRGN	bit chart 3→0 : MPBRGN Table 3.118 MPBRGN Register Contents Bit Position : 31 to 4 – 3 to 0 MPBRGN	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	Modified the section title of No.12.	298	260	253
53	298	CPU System	(4) MPTRGN – MPU end region register @PCU	bit-map 4→0 : MPTRGN Table 3.119 MPTRGN Register Contents Bit Position : 31 to 5 – 4 to 0 MPTRGN	bit-map 3→0 : MPTRGN Table 3.119 MPTRGN Register Contents Bit Position : 31 to 4 – 3 to 0 MPTRGN	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	Modified the section title of No.13.	298	260	253
54	582	CSIH	13.5.10 CSIH interrupt requests (3) INT_CSIHTIC (communication status interrupt) Figure 13.25 Generation of INT_CSIHTIC in Job Mode			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		582	543	534
55	583	CSIH	13.5.10 CSIH interrupt requests (3) INT_CSIHTIC (communication status interrupt) Table 13.10 Generation of INT_CSIHTIC in Job Mode	 CSIHnTX0W.CSIHnEOJ / INT_CSIHTIC 0 Not generated 0 Generated 1 Not generated 1 CSIHnCTL0.CSIHnJOBE = 0: Generated CSIHnCTL0.CSIHnJOBE = 1: Not generated, replaced by interrupt INT_CSIHTUC	The left descriptions maked in red are deleted. CSIHnTX0W.CSIHnEOJ / INT_CSIHTIC 0 Generated 1 CSIHnCTL0.CSIHnJOBE = 0: Generated CSIHnCTL0.CSIHnJOBE = 1: Not generated, replaced by interrupt INT_CSIHTUC	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		583	544	535
56	860	RS-CAN	16.4.2.6 Channel Modes Figure 16.5 Channel Mode State Transition Chart	Refer to "No.56_Figure 16.5" Sheet.	Refer to "No.56_Figure 16.5" Sheet.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		860	821	812
57	861	RS-CAN	16.4.2.7 Channel Stop Mode	In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.	In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited (except write to the CSLPR bit). Register values are retained.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		861	822	813
58	903	RS-CAN	Figure 16.36 RAM Test Setting Procedure	RSCANOGTSTCTR register RTME bit ←1	・RSCANOGTSTCTR register RTME bit ←1 *1 ・The following descriptions are added on the bottom of the chart. Note 1. Before changing to the RAMTEST mode, make sure to: ・Cancel transmission request(s), if any. ・Disable all the FIFO and Transmit Queues, and. ・Clear the receiving flags of receiving buffers.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		903	864	855
59	952	FlexRay	17.2.5.3 FLXAOFRT2C – FlexRay Timer 2 Configuration Register	17.2.5.3 FLXAOFRT2C – FlexRay Timer 2 Configuration Register Access: This register can be read/written in 8-, 16-, or 32-bit units.	17.2.5.3 FLXAOFRT2C – FlexRay Timer 2 Configuration Register This register is an absolute timer. Timer 2 has the same absolute timer features as timer 0. Access: This register can be read/written in 8-, 16-, or 32-bit units.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		952	913	–
60	1177	FlexRay	17.3.16.3 Data Structure Transfer Scheduling (1) All dedicated message buffers in ascending order	・FLXAOFRNDATn (2 places) ・FLXAOFRMBSCn	・FLXAOFRNDATn→ FLXAOFRNDATi (2 places) ・FLXAOFRMBSCn→ FLXAOFRMBSCi	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1177	1138	–
61	1404	ATU-IV	21.4.2.8 TIOR2A – Timer I/O Control Register 2A (1) NZKGA0 to 6 – Noise Canceler Clock Select G A0 to 6	E1x-FCC1, E1M-S: These bits select the count source clock of noise canceler counters A0 to 6 (NCNTGA0 to 6). E1L: These bits select the count source clock of noise canceler counters A0 to 5 (NCNTGA0 to 5).	E1x-FCC1, E1M-S: These bits select the count source clock of noise canceler counters A0 to 6 (NCNTA0 to 6). E1L: These bits select the count source clock of noise canceler counters A0 to 5 (NCNTA0 to 5).	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	Added E1L information to No. 29.	1404	1365	1065
62	1951	TSG2	Figure 23.15 Interrupt Generation Example (1/2) (Example of HT-PWM Mode)			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".	Added corrections of INTTSG 2nI[5], [6], [9], [10] to No. 35.	1951	1912	1611
63	2010	TSG2	23.11.2.8 Notes Concerning Dead Time Control in HT-PWM Mode (1) TSG2nDTCO and TSG2nDTC1 Rewriting CAUTIONS 3			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2010	1971	1670
64	2010	TSG2	23.11.2.8 Notes Concerning Dead Time Control in HT-PWM Mode (1) TSG2nDTCO and TSG2nDTC1 Rewriting CAUTIONS 4			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2010	1971	1670
65	2123	ADCB	26.5.2 ADCBmDRn – Data Register n	N/A	The following descriptions are added above the NOTE. CAUTIONS 1. Note that an unintended parity error may occur when ADCBmDRi or ADCBmDRi + 1 where an A/D converted value is stored is read after any one of the following procedures (i) to (iii) is executed and before the A/D converted value is updated. (i) The set value of ADCBmADCR2.ADDNT is changed (ii) The set value of ADCBmVCRn.CNVCLS [2: 0] in the corresponding scan group is changed from any of 0H, 1H, 2H, 3H, or 5H to 4H or 6H (iii) The set value of ADCBmVCRn.CNVCLS [2: 0] in the corresponding scan group is changed from 4H or 6H to any of 0H, 1H, 2H, 3H, or 5H 2.For ADCBmDRn reading, ADCBmDRi and ADCBmDRi + 1 are to be read when 16-bit read access occurs in ADCBmDRi or ADCBmDRi + 1. When any one of (i) to (iii) in Caution 1 is executed after scan group completion and a scan group is executed again while ADCBmSFTCR.RDCLRE = 0, reading ADCBmDRi in 16- or 32-bit units before an A/D converted value is stored in ADCBmDRi + 1 may result in an unintended parity error.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2123	2084	1777

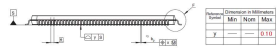
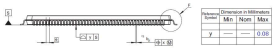
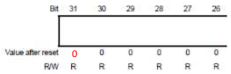
Errata of RH850/E1x User's Manual Hardware Rev.1.20
The changes are shown below. (Error: red, Correct: blue)
PDF page (Rev.x.xxE) lists representative product E1x-FCC1. For details, refer to "UM (page) that applies the same correction" column.

No.	PDF Page (Rev.x.xxE)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note	UM (page) that applies the same correction: E1x-FCC1	E1M-S	E1L
66	2563	Flash Memory	Table 33.9 FRDCYCLD Register Contents	N/A	Note : read cycle is 40MHz, In this products.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2563	2524	2201
67	2605	Electrical Characteristics	Table 37.2 Relationship between Power Name and Pin	PinName | ～ | I/O | Max. InputVoltage(V) | InputBufferType TDO/LPDO/FLSCI3TX | ～ | O | VCC+0.3 | TTL2 DRDY/LPDCLKO | ～ | O | VCC+0.3 | TTL2	PinName | ～ | I/O | Max. InputVoltage(V) | InputBufferType TDO/LPDO/FLSCI3TX | ～ | O | — | — DRDY/LPDCLKO | ～ | O | — | —	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2605	2564	2239
68	481, 483	Power Supply Circuit	9.5 Guide to Mounting on Boards with an EPT 9.5.1 QFP 9.5.2 BGA CAUTIONS (E1M-Sは、9.5.1 BGA)	1. Values for the parasitic L and R components produced by connection of VSS are based on the assumption that VSS is supplied through a plane of the board (with copper thickness of 35 μm and pitch of at least 1 mm for both VSS and VDD).	1. Values for the parasitic L and R components produced by connection of VSS are based on the assumption that VSS is supplied through a plane of the board (with copper thickness of 35 μm and pitch of at most 1 mm for both VSS and VDD).	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		481, 483	444	434, 436
69	719	RS-CAN	Table 16.2 Index	For example, a transmit/reception FIFO buffer configuration/control register is written as RSCANOCFCCk (k = 0 to 14).	For example, a transmit/reception FIFO buffer configuration/control register is written as RSCANOCFCCk (k = 0 to 11).	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		719	680	671
70		RS-CAN	Only Japanese UM is modified.								
71	778	RS-CAN	16.3.2.15 RSCANOGAFLPOj – Receive Rule Pointer O Register (j = 0 to 15)	GAFLRMDP[6:0] Bits These bits are used to select the number of a receive buffer that stores received messages having passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than the value set by the NRXMB[7:0] bits in the RSCANORMNB register.	GAFLRMDP[6:0] Bits These bits are used to select the number of a receive buffer that stores received messages having passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than the setting value by the NRXMB[7:0] bits in the RSCANORMNB register.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		778	739	730
72	861	RS-CAN	16.4.2.7 Channel Stop Mode	In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.	In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. Channel related registers can be read, but writing data to them is prohibited (except write to the CSLPR bit). Register values are retained.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		861	822	813
73	E1L only (UM P1049)	ATU-IV	21.4.1 Operation	～Six event signals TIAO0 to O5 are output (event outputs 1B to 1H) ～	～Six event signals TIAO0 to O5 are output (event outputs 1B to 1G) ～	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1049
74	E1L only (UM P1050)	ATU-IV	Figure 21.6 Timer A Block Diagram	Event output 1B to 1H	Event output 1B to 1G	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1050
75	E1L only (UM P1086)	ATU-IV	21.5.1 Operation Edge-Interval Measuring Block	In the edge-interval measuring block, the event counter B1(TCNTB1) value is captured for the event counter B1(TCNTB1) at occurrence of any of seven external event input signals 1B to 1H that are input via timer A (ICRB30 to ICRB36). The event counter B1(TCNTB1) is not cleared at occurrence of any of external event input signals 1B to 1H.	In the edge-interval measuring block, the event counter B1(TCNTB1) value is captured for the event counter B1(TCNTB1) at occurrence of any of six external event input signals 1B to 1G that are input via timer A (ICRB30 to ICRB35). The event counter B1(TCNTB1) is not cleared at occurrence of any of external event input signals 1B to 1G.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1086
76	E1L only (UM P1088)	ATU-IV	Figure 21.15 Timer B Block Diagram	Event input 1H ——→ ICRB36	Event input 1G ——→ ICRB35	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1088
77	E1L only (UM P1105)	ATU-IV	21.5.2.10 ICRB3x	Input capture registers B30 to B36 (ICRB30 to ICRB36) are 8-bit read-only registers. In the edgeinterval measuring block, the event counter B1 (TCNTB1) value is captured at occurrence of any of seven external event inputs 1B to 1H that are input via timer A (ICRB30 to ICRB36). The event counter B1 (TCNTB1) is not cleared at occurrence of any of external event inputs 1B to 1H. ICRB30 to ICRB36 can be read only in 8-bit units. ICRB30 to ICRB36 are initialized to 00H by a reset.	Input capture registers B30 to B36 (ICRB30 to ICRB35) are 8-bit read-only registers. In the edgeinterval measuring block, the event counter B1 (TCNTB1) value is captured at occurrence of any of six external event inputs 1B to 1G that are input via timer A (ICRB30 to ICRB35). The event counter B1 (TCNTB1) is not cleared at occurrence of any of external event inputs 1B to 1G. ICRB30 to ICRB36 can be read only in 8-bit units. ICRB30 to ICRB36 are initialized to 00H by a reset. Note : E1L don't use ICRB36 because external event inputs / outputs 1H is not suport.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1105
78	E1L only (UM P1138)	ATU-IV	21.5.3.1 Edge Interval Measuring Function and Edge Input Stopping Function	Registers ICRB30 to ICRB 36 capture the TCNTB1 value by using the external event input 1B to 1H as a trigger. ICRB30 corresponds to external event input 1B and ICRB31 to ICRB36 correspond to respective external event input 1C to 1H.	Registers ICRB30 to ICRB 35 capture the TCNTB1 value by using the external event input 1B to 1G as a trigger. ICRB30 corresponds to external event input 1B and ICRB31 to ICRB35 correspond to respective external event input 1C to 1G.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1138
79	E1L only (UM P1139)	ATU-IV	Figure 21.18 Count Operation of TCNTB1 and Capture Operation of ICRB3x	Event input 1H (5 places) ICRB36	Event input 1G (5 places) ICRB35	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1139
80	E1L only (UM P1200)	ATU-IV	21.7.1 Operation Overview	Each channel includes two output pins: TODxyA for compare match output and TODxyB for one-shot pulse output. (Output pins are supported by subblocks D0 to D8.)	Each channel includes two output pins: TODxyA for compare match output and TODxyB for one-shot pulse output. (Output pins are supported by subblocks D0 to D4.)	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1201
81	1548	ATU-IV	21.7.2.3 TIOR1Dx (2) IOADxy[1:0] – I/O Control A	～ a signal is output on pin TODxyA according to the IOADxy bits (only subblocks D0 to D9).	～ a signal is output on pin TODxyA according to the IOADxy bits (only subblocks D0 to D8).	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		1548	1509	–
82		ATU-IV	Only Japanese UM is modified.								
83		ATU-IV	Only Japanese UM is modified.								
84		ATU-IV	Only Japanese UM is modified.								
85		ATU-IV	Only Japanese UM is modified.								
86	2085	PIC	25.2.3.3 PIC2ADTEN5nj	bit box bit31 – 16 R/W R – R	bit box bit31 – 16 R/W R/W – R/W	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2085	2046	–
87	E1L only (UM P1743)	PIC	25.2.3.3 PIC2ADTEN5nj	bit box bit23 – 16 R/W R – R	bit box bit23 – 16 R/W R/W – R/W	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	1743
88		PIC	Only Japanese UM is modified.								
89	2329	Safety	29.2.3.2 List of Registers (1) List of ECC Modules Table 29.16 List of Modules	Master Side | Checker Side	Master Side*1 | Checker Side*1 Note 1. Two ECC modules are provided to support BIST, one for the master and the other for the checker. For details, refer to Section 29.7, BIST.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2329	2290	1983
90	2318	Safety	Table 29.5 CFAPCTL Register Contents Bit Position 2	Address Parity Checker (Bank B) Test	Address Parity Checker (Bank B) Test This product does not use this bit.	Additional Description	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2318	2279	1972
91	2430	Safety	29.3 Lockstep	N/A	29.3.3 Usage Notes Reading a register with a value that is undefined after a reset without initializing the register may lead to a lock step compare error. Accordingly, such registers must be initialized with the desired settings. Even if the branch instruction and the subsequent instruction is issued in parallel, the lock step compare error might be occurred by undefined register after the reset. It should be applied as specified below until the register which refer by subsequent instruction is initialized in case of branching in the preceding instruction. -Insert the NOP instruction, the SYNCI instruction , or the RIE instruction following the branch instruction. (It has to be added by assembler language. When C language is used, it could be optimized.) -Applicable branch instructions: Bcond, JARL, JMP, JR	Description Change	Reported on TECHNICAL UPDATE "TN-RH8-B0183C/E"(Rev.3) and "TN-RH8-B111C/E".		2430	2391	2084
92	2538	OCD	Table 32.2 I/O Pins of AUDR			Description Change	Reported on TECHNICAL UPDATE "TN-RH8-B0228A/E" and "TN-RH8-B111C/E".		2538	2499	–
93	2549	OCD	32.5.4.3 Usage Notes on AUDR Function			Description Change	Reported on TECHNICAL UPDATE "TN-RH8-B0228A/E"and "TN-RH8-B111C/E".		2549	2510	–
94	2550	Flash Memory	33.1 Features	· Support for protection functions to protect against erroneous overwriting of the flash memory	· Support for protection functions to protect against erroneous programming/erasure of the flash memory	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2550	2511	2188

Errata of RH850/E1x User's Manual Hardware Rev.1.20

The changes are shown below. (Error: red, Correct: blue)

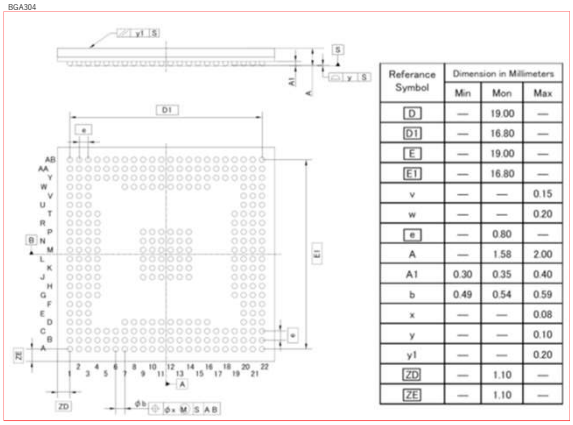
PDF page (Rev.x.xxE) lists representative product E1x-FCC1. For details, refer to "UM (page) that applies the same correction" column.

No.	PDF Page (Rev.x.xxE)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note	UM (page) that applies the same correction		
									E1x-FCC1	E1M-S	E1L
95	2571	Flash Memory	33.11 Usage Notes (3) Prohibition of additional writing	Writing to a given area twice is not possible. If you want to overwrite data in an area of flash memory after writing to the area has been completed, erase the area first.	Writing to a given area twice is not possible. If you want to update data in an area of flash memory after writing to the area has been completed, erase the area first.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2571	2532	2209
96	2571	Flash Memory	33.11 Usage Notes (4) Resets during programming and erasure	In the case of an internal or external reset during programming and erasure, wait for at least the minimum width of reset pulse once the operating voltage is within the range stipulated in the electrical characteristics before releasing the device from the reset state.	In the case of an external reset during programming and erasure, wait for at least the minimum width of reset pulse once the operating voltage is within the range stipulated in the electrical characteristics before releasing the device from the reset state.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2571	2532	2209
97	E1L only (UM P2277)	Electrical Characteristics	Table 37.35 ADC Converter Characteristics	Digital resolution Typ. 2	Digital resolution Typ. 12	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	2277
98	E1L only (UM P2284)	Electrical Characteristics	Table 37.44 JESD51-9 Compliant Board (4 layers)	L Board | 101.5 | 114.5 | 11621.75	Board | 101.5 | 114.5 | 11621.75	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		–	–	2284
99	2617	Electrical Characteristics	37.2.11 Supply Current Characteristics	CAUTIONS 1. When the A/D converter is not used or it is in the standby state, do not open the AOVCC pin, AIVCC pin, AOVREFH pin, AIVREFH pin, ADSVREFH pin, ADSVREFL pin, AOVSS pin, and AIVSS pin.	CAUTIONS 1. Even if the A/D converter is not used or it is in the standby state, do not open the AOVCC pin, AIVCC pin, AOVREFH pin, AIVREFH pin, ADSVREFH pin, ADSVREFL pin, AOVSS pin, and AIVSS pin.	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2617	2576	2251
100	2629	Electrical Characteristics	Figure 37.12 CSIH Timing (Master Mode)	CSIHnCFGx*	CSIHnCFGx	Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B111C/E".		2629	2588	2263
101	2855	Appendix Package Dimensions	Appendix Package Dimensions			Writing Error	Reported on TECHNICAL UPDATE "TN-RH8-B163A/E" and "TN-RH8-B111C/E".		2855	–	2452
102	787	RS-CAN	16.3.2.23 RSCANORFCCx – Receive FIFO Buffer Configuration/Control Register (x = 0 to 7)	RFE Bit Setting the RFE bit to 1 makes receive FIFO buffers available. Clearing this bit to 0 sets the RFEMP flag in the RSCANORFSTSx register to 1 (the receive FIFO buffer contains no unread message (buffer empty)). Modify this bit in global operating mode or global test mode.	RFE Bit Setting the RFE bit to 1 makes receive FIFO buffers available. Clearing this bit to 0 sets the RFEMP flag in the RSCANORFSTSx register to 1 (the receive FIFO buffer contains no unread message (buffer empty)). Modify this bit in global operating mode or global test mode. After all other bits in the RSCANnRFCCx register have been set, set this bit to 1 by using another instruction. This bit is set to 0 in global reset mode.	Additional Description			787	748	739
103	798	RS-CAN	16.3.2.30 RSCANOCFCCk – Transmit/Receive FIFO Buffer Configuration/Control Register (k = 0 to 11)	CFE Bit Modify this bit in the following mode. · Receive mode: Global operating mode or global test mode · Transmit mode or gateway mode: Channel communication mode or channel halt mode	CFE Bit Modify this bit in the following mode. · Receive mode: Global operating mode or global test mode · Transmit mode or gateway mode: Channel communication mode or channel halt mode After all other bits in the RSCANnCFCCk register have been set, set this bit to 1 by using anotherinstruction.	Additional Description			798	759	750
104	879	RS-CAN	16.4.6.6 RAM Test	The RAM test function allows accesses to all CAN RAM addresses. RAM initialization which is performed after resetting the MCU does not initialize all CAN RAM areas. When the RAM test function is used, the RAM is divided into pages of 256 bytes each. A RAM test page is selected by the RTMPS[6:0] bits in the RSCANOGTSTCFG register. Data in the set page can be read from and written to the RSCANORPGACCr register (r = 0 to 63). The available total RAM size is 12160 bytes (2F80H).	The RAM test function allows accesses to all CAN RAM addresses. RAM initialization which is performed after resetting the MCU does not initialize all CAN RAM areas. When the RAM test function is used, the RAM is divided into pages of 256 bytes each. A RAM test page is selected by the RTMPS[6:0] bits in the RSCANOGTSTCFG register. Data in the set page can be read from and written to the RSCANORPGACCr register (r = 0 to 63). The available total RAM size is 12160 bytes (2F80H). Do not access more than 128 bytes in the last page (RTMPS[6:0] = 2FH) during RAM test.	Additional Description			879	840	831
105		ATU-IV	Only Japanese UM is modified.								
106	1867	APA	22.5.7.2 Matching Condition Setting 2 (ADC Input)	In cases where the reference input takes discrete values (e.g. ADC), matching condition specification (APAAELMMCON[1:0] or APAAELMMCOFF[1:0]) should use ">" or "<" (because "==" specification might not have matches as expected).	In cases where the reference input takes discrete values (e.g. ADC), matching condition specification (APAAELMMCON[1:0] or APAAELMMCOFF[1:0]) recommend use ">" or "<" (because "==" specification might not have matches as expected).	Writing Error			1867	1828	1528
107	2248	DFE	28.2.5 PHCHn – PH Result Register (n = 0 to 9)			Writing Error			2248	2209	1902
End of Column											

Package Dimensions(BGA)

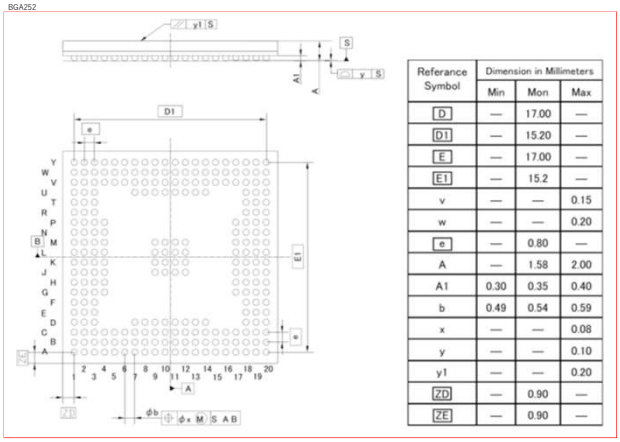
Before

BGA304



Referance Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	19.00	—
D1	—	16.80	—
E	—	19.00	—
E1	—	16.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

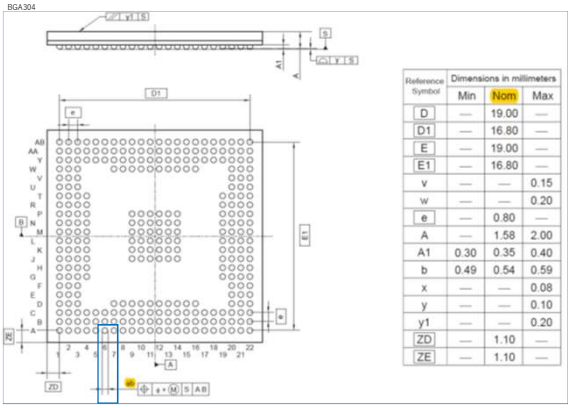
BGA252



Referance Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	17.00	—
D1	—	15.20	—
E	—	17.00	—
E1	—	15.2	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	0.90	—
ZE	—	0.90	—

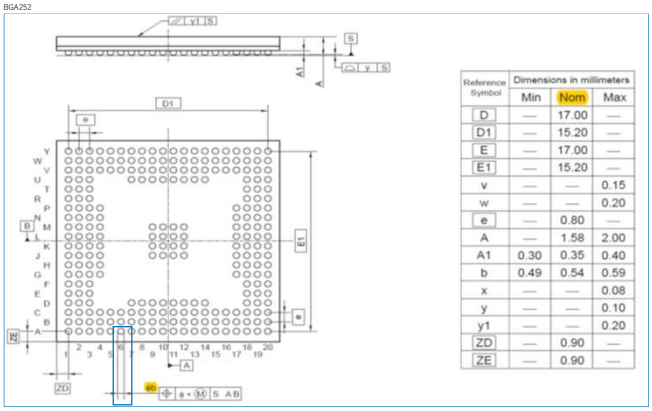
After

BGA304



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	19.00	—
D1	—	16.80	—
E	—	19.00	—
E1	—	16.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

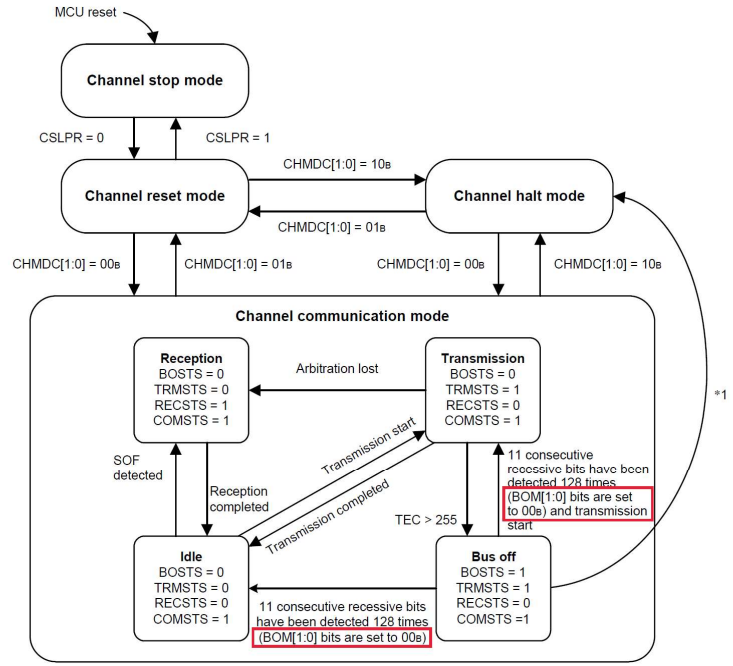
BGA252



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	17.00	—
D1	—	15.20	—
E	—	17.00	—
E1	—	15.20	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	0.90	—
ZE	—	0.90	—

No.56_Figure 16.5

Before

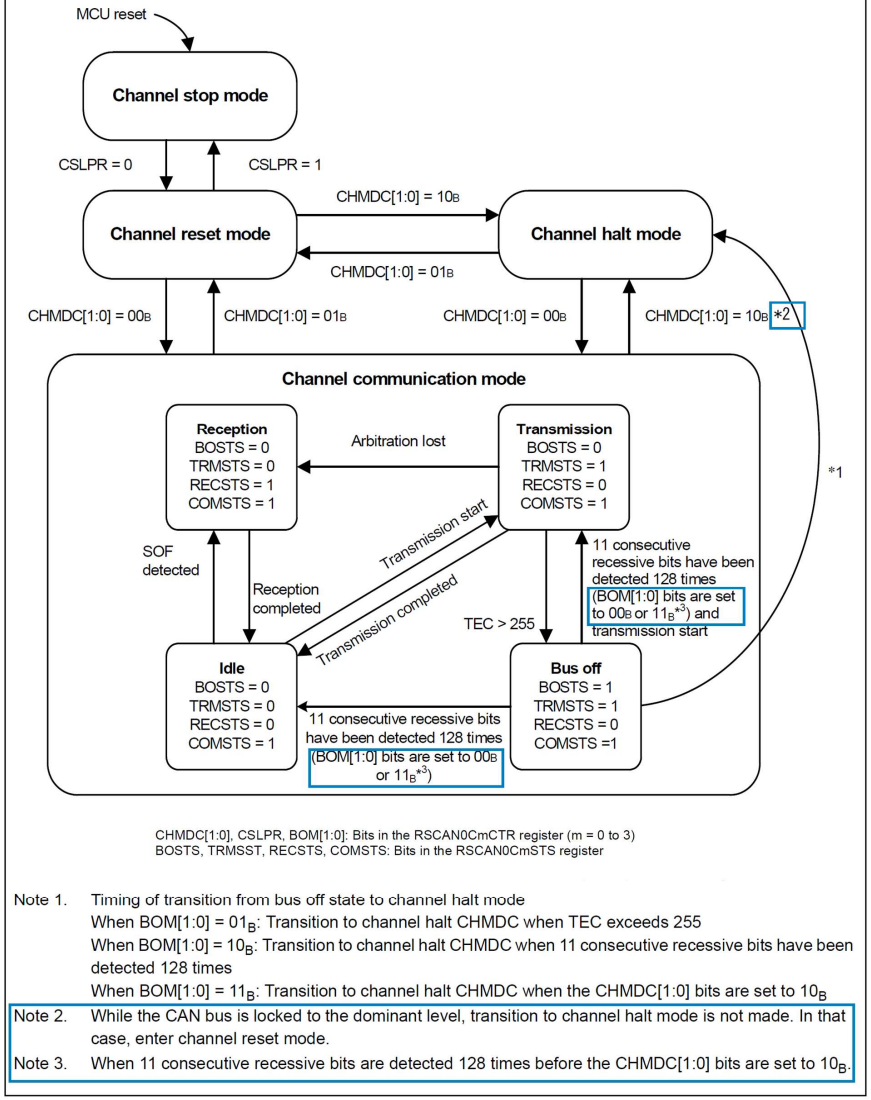


CHMDC[1:0], CSLPR, BOM[1:0]: Bits in the RSCAN0CmCTR register (m = 0 to 3)
BOSTS, TRMSST, RECSTS, COMSTS: Bits in the RSCAN0CmSTS register

Note 1. Timing of transition from bus off state to channel halt mode
When BOM[1:0] = 01_B: Transition to channel halt CHMDC when TEC exceeds 255
When BOM[1:0] = 10_B: Transition to channel halt CHMDC when 11 consecutive recessive bits have been detected 128 times
When BOM[1:0] = 11_B: Transition to channel halt CHMDC when the CHMDC[1:0] bits are set to 10_B

Figure 16.5 Channel Mode State Transition Chart

After



CHMDC[1:0], CSLPR, BOM[1:0]: Bits in the RSCAN0CmCTR register (m = 0 to 3)
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When BOM[1:0] = 11_B: Transition to channel halt CHMDC when the CHMDC[1:0] bits are set to 10_B

Note 2. While the CAN bus is locked to the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode.

Note 3. When 11 consecutive recessive bits are detected 128 times before the CHMDC[1:0] bits are set to 10_B.

Figure 16.5 Channel Mode State Transition Chart