CUSTOMER NOTIFICATION

SUD-DT-04-0197 (1/7)
April 23, 2004

Koji Nishibayashi, Senior System Integrator
Microcomputer Group
2nd Solutions Division
Solutions Operations Unit
NEC Electronics Corporation

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IE-703217-G1-EM1

(Control Code: A, B, C, D)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-703217-G1-EM1

1. Product Version

Control Code[Note]	Board Version	Marking on Peripheral EVA Chip
A	V1.00	D70F3217Y DS1.1
B	V1.20	D703217 ES1.4
C	V1.30	D70F3217 DS2.1
D	V1.40	D703217GJ-ICE

Employ an IE-V850ES-G1 with a control code of C or later when using this emulation board.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]			
		A	B	C	D
1	ROM correction function cannot be emulated	Permanent restriction			
2	Restriction on ROM correction	×	√	√	√
3	Restriction on use-prohibited area	Permanent restriction			
4	Restriction on D/A converter	×	√	√	√
5	Restriction on interrupt request flag	×	√	√	√
6	Restriction on IIC bus communication reservation	×	×	√	√
7	Restriction on transmit data write using 3-wire serial interface with automatic transfer function	×	×	√	√
8	Restriction on I/O register access when VSWC register = 0x00	×	×	×	√

×: Applicable, √: Not applicable or already corrected

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

3. Details of Bugs and Added Specifications

No.1 ROM correction function cannot be emulated

[Description]

The ROM correction function cannot be emulated.

[Workaround]

There is no workaround.

No.2 Restriction on ROM correction

[Description]

Correction address registers 0 to 3 (CORAD0 to CORAD3) and the correction control register (CORCN) cannot be read/written correctly.

[Workaround]

This restriction has been corrected in control code B.

No.3 Restriction on use-prohibited area

[Description]

A fail-safe break does not occur even if the program is executed or an access occurs in 0x3FFC000 to 0x3FFDFFF (device with 6 KB internal RAM: 0x3FFC000 to 0x3FFD7FF) in the use-prohibited area of the target device.

[Workaround]

Regard this as a permanent restriction.

A break can be generated when the program is executed or an access occurs by setting a break on the debugger under the following conditions.

♦ Device with 4 KB internal RAM

- Detects program execution at 0x3FFC000 to 0x3FFDFFF
  - Event status: Execution
  - Address: 0x3ffc000 to 0x3ffdfff

  (Two execution events are used by setting the above conditions.)
- Detects access for 0x3FFC000 to 0x3FFDFFF
  - Event status: R/W
  - Access size: No Condition
  - Address: 0x3ffc000 to 0x3ffdfff

  (Two access events are used by setting the above conditions.)

♦ Device with 6 KB internal RAM

- Detects program execution at 0x3FFC000 to 0x3FFD7FF
  - Event status: Execution
  - Address: 0x3ffc000 to 0x3ffd7ff

  (Two execution events are used by setting the above conditions.)

- Detects access for 0x3FFC000 to 0x3FFD7FF
  - Event status: R/W
  - Access size: No Condition
  - Address: 0x3ffc000 to 0x3ffd7ff

    (Two access events are used by setting the above conditions.)

No.4 Restriction on D/A converter

[Description]

When AV_{REF1} is used at less than 3.0 V, the D/A conversion value cannot be guaranteed.

(A D/A converter is not provided in the V850ES/KF1.)

[Workaround]

Use the D/A converter with AV_{REF1} = 3.0 V or higher. ($V_{DD} \geq AV_{REF1}$)

This restriction has been corrected in control code B.

No.5 Restriction on interrupt request flag

[Description]

The interrupt request flag is not cleared even if an interrupt request has been acknowledged.

[Workaround]

Add processing to clear the interrupt request flag at the beginning of the handler address of the acknowledged interrupt. Clearance of the interrupt request flag can be performed by instruction execution.

This restriction has been corrected in control code B.

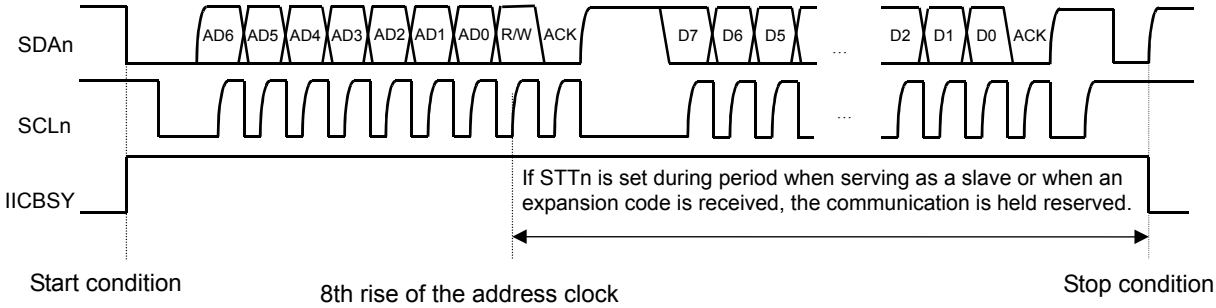
No.6 Restriction on IIC bus communication reservation

[Description]

If conditions (1) and (2) are satisfied when using the IIC bus interface (IICn), the communication is held reserved even if communication reservation is disabled (IICRSVn = 1). At this time, the start condition clear flag (STCFn) is not set (n = 0 or 1). (See the figure below.)

(1) When the address value and the slave address register (SVAn) value match or when an expansion code is received

(2) When the start condition trigger (STTn) is set in the period from the 8th rise of the address clock to stop condition detection.



[Workaround]

This bug can be avoided by software.

This bug occurs when the bus flag (IICBSY) is being set. Before generating the start condition (STTn ← 1) while communication reservation is disabled (IICRSVn = 1), confirm that the IIC bus status flag has been cleared (IICBSYn = 0).

STTn can be set immediately after IICBSYn = 0 is confirmed, but it is recommended to disable interrupts because if it takes a long time to set STTn due to an interrupt, the start condition may be detected during the period, and a slave match may occur or expansion code may be received at the 8th address clock.

This restriction has been corrected in control code C.

No.7 Restriction on transmit data write using 3-wire serial interface with automatic transfer function

[Description]

When writing transmit data to the buffer RAM (CSIAnBm) using the 3-wire serial interface with automatic transfer function (CSIAn), data may not be written correctly depending on the instruction executed next to the write instruction (n = 0 or 1, m = 0 to F).

This restriction is not applicable under the following condition.

Condition: CSIAn input clock (f_{SCKA}) is faster than the CPU operating clock (fcpu) × 10

$$fcpu \times 10 < f_{SCKA}$$

f_{SCKA}: CSIAn input clock selected by bits 6 and 7 (CKSAn0 and CKSAn1) of the CSIAn status register (CSISn)

[Workaround]

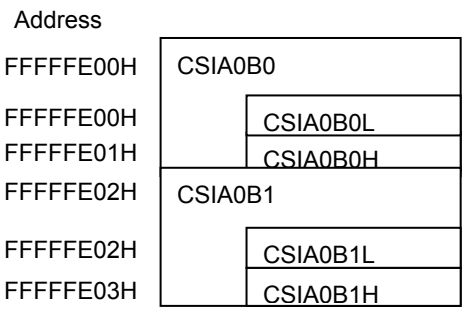
Implement any of the workarounds shown below by software. To avoid this restriction, it is required to use instructions with the same access length until the write is complete.

Workaround (1)

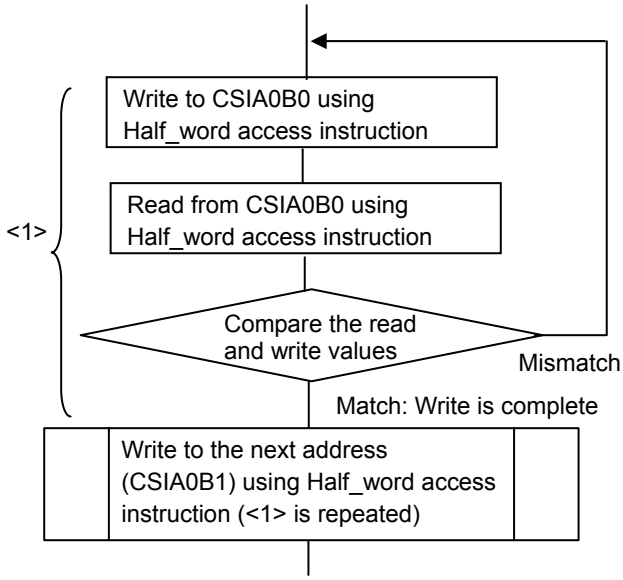
After data is written, read the data using the Half_Word access instruction (ST.H) and compare the values. If the data do not match, perform the write again. At this time, it is not necessary to disable interrupts.

When writing an odd number of bytes, write dummy data to the buffer RAM (CSIAnBmH) at the higher address. The Half_Word access instruction must be used to access registers until the compare result matches and write is confirmed.

<Example of writing to buffer RAM (CSIA0B0 to CSIA0B1)>



Buffer RAM configuration



<Example of writing only 1-byte data (to CSIA0B0L)>

Perform operation <1> to write data to CSIA0B0L, by writing dummy data to CSIA0B0H (the buffer RAM at the higher address).

Workaround (2)

Disable interrupts using the DI instruction and write data to the buffer RAM using the Half_Word access instruction (ST.H) only. In addition, re-write the last 2 bytes of the written data again. Do not execute instructions other than NOP and operation instructions between when data is written to the buffer RAM and when the last 2 bytes are rewritten.

When writing an odd number of bytes, write dummy data to the buffer RAM (CSIAnBmH) at the higher address.

Workaround (3)

Disable interrupts using the DI instruction and write data to the buffer RAM using the byte access instruction (ST.B) only. In addition, execute a NOP or operation instruction equivalent to 5 or more input clocks selected by bit 6 and 7 (CKSAn1 and CKSAn0) of CSISn after the last data is written to the buffer RAM.

This restriction has been corrected in control code C.

No.8 Restriction on I/O register access when VSWC register = 0x00

[Description]

An access to the I/O register may be illegal when the VSWC register is set to 0x00 and used at an operating frequency of 13.0 to 16.6 MHz. In the case of a write access, an unexpected value is written. In the case of a read access, an illegal value is read.

[Workaround]

Set the VSWC register to 0x01 when using at an operating frequency of 13.0 to 16.6 MHz.

This restriction has been corrected in control code D.

4. Cautions

No.1 Caution on ID703000 (ID850)

[Description]

Use V2.51 or later when using the IE-703217-G1-EM1 with the NEC Electronics debugger.

5. Revision History

Document Number	Issued on	Description
SUD-TT-0117-2-E	May 13, 2002	Newly created.
SUD-TT-0117-4-E	July 26, 2002	Addition of new bug (No.5)
SUD-DT-03-0136-1-E	March 20, 2003	Addition of new bugs (No.6 and No.7)
SUD-DT-04-0197	April 21, 2004	Addition of new bug (No.8)