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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A871A/E	Rev.	1.00
Title	Manual correction about the control register of SCIF of SH7730		Information Category	Technical Notification		
Applicable Product	SH7730 group	Lot No. All	Reference Document	SH7730 Group User's Manual: Hardware (R01UH0346EJ0400) Rev. 4.00		

It corrects about the MCE of FIFO Control Register (SCFCR) of the Serial Communication Interface with FIFO(SCIF) of the SH7730 hardware manual.

[Error] Page 704 of 1162,Section 22 22.3.9 FIFO Control Register (SCFCR)

Bit	Bit Name	Initial Value	R/W	Description
3	MCE	0	R/W	Modem Control Enable Enables modem control signals $\overline{CTS}$ and $\overline{RTS}$. In clock synchronous mode, MCE bit should always be 0. 0: Modem signal disabled* 1: Modem signal enabled Note: * $\overline{CTS}$ is fixed at active 0 regardless of the input value, and $\overline{RTS}$ is also fixed at 0.

[Correction]

Bit	Bit Name	Initial Value	R/W	Description
3	MCE	0	R/W	Modem Control Enable Enables modem control signals $\overline{CTS}$ and $\overline{RTS}$. In clock synchronous mode, MCE bit should always be 0. 0: Modem signal disabled* 1: Modem signal enabled Note: * $\overline{CTS}$ is fixed at active 0 regardless of the input value, and $\overline{RTS}$ enter high impedance state..