Date: Oct. 21, 2013

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A877A/E	Rev.	1.00
Title	Notes about the RES_F_HW[10:0] bits in the Full-Screen Horizontal Size Register(SCL0_FRC7) of Video Display Controller 4.		Information Category	Technical Notification		
Applicable Product	SH7268 Group SH7269 Group	Lot No. ALL	Reference Document	SH7268 Group, SH7269 Group User'sManual: Hardware Rev2.00 (R01UH0048EJ0200)		

We would like to inform you of the following notice about the RES_F_HW [10:0] bits in the Full-Screen Horizontal Size Register (SCL0_FRC7) when Serial RGB Output for LCD output signal is selected.

[Description of the RES_F_HW [10:0] bits]

Horizontal Enable Signal Width for Full Screen (pixel-clock cycles)

Note: RES_F_HS + RES_F_HW should be equal to or less than 2015(clock cycles).

Note 2: When Serial RGB Output for LCD output signal is selected, these bits are set to (Horizontal Enable Signal Width for Full Screen + 2).