RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A920A/E	1.00		
Title	Notes about SSCG		Information Category	Technical Notification			
Applicable Product	See following	Lot No.					
		All	Reference Document	See following			

In the products listed in bellow, a bug about SSCG function is found. There is a possibility that SSCG function can not modulate clock frequency properly.

The details is shown in below.

Applicable products and relevant documents

Applicable products		Relevant documents		Document number	
series	Group				
SH7260	SH7268,	SH7268 Group, SH7269 Group	Rev	R01UH0048EJ0300	
	SH7269	User's Manual: Hardware	3.00		

[1] Condition

When SSCG is used and fulfill more than one of following conditions.

- The power is supplied in the power on sequence as following order
 - 1) Supply 3.3 volt power and MD_CLK0 pin is changed to high level (SSCG ON)
 - 2) Supply 1.2 volt power

Detail condition is described in "[4] Detail Condition".

[2] Phenomenon

There is a possibility that clock modulation function does not work and the frequency is fixed to the lower limit frequency.





[3] Workaround

Please apply the following software workarounds or hardware workarounds.

• Software workarounds

After power on, be sure to execute transition to Deep standby mode and cancelling, then execute user program.

Details are described in the "[5] Software workarounds details".

- Hardware workarounds
- Please make more than one microsecond between Vcc power on and change timing of MD_CLK0 pin to high level. (below figure)



- PVcc power on timing should be at the same time as MD_CLK0 pin or faster than MD_CLK0 pin. (below figure)

if PVcc power on timing is later than change timing of MD_CLK0 pin to high level, it becomes absolute maximum rating violation.









[5] Software workarounds details

According to flowchart below, after power on, be sure to execute transition to Deep standby mode and cancelling, then execute user program.

Program Start	
Judge whether Deep standby mode after power on by RTCARF bit of De (When RTCARF = 1, cancelled from	e cancellation process or power on reset process eep standby cancel source flag register (DSFR) n Deep standby mode)
From power on Yes, from power	ver on reset
(RTCARF == 0?)	
No. Cancelled from Deep	
standby mode	Initialize RTC and transition to Deep standby mode
Clear IOKEEP bit	(Set RTC alarm 1ms)
Stop RTC *1	
Initialize peripheral function Execute user program (Cancell	e this improper phenomenon can be solved by ning and cancelling to/from Deep standby mode, e transition to Deep standby mode only once wer on reset. ling factor: RTC alarm interrupt)
*1: Please execute depending on system	
Only when selecting EXTAL as RTC operation clock, one-second counting operation can be set by Frequer	, the frequency of the operation clock for performing t ncy register H / L (RFRH / L).
In this case, by setting the value of RFRH / L re	gister according to the following formula, RTC ala
interrupt can be generated in less than 1s.	
RFRH/L.RFC[18:0] = Alarm interrupt time ÷ (EXTA (in case of RFRH/L.SEL64 = 1)	AL period × 64)
e.g.) When EXTAL frequency is 13.33MHz, RFC[18:0]] =209

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