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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0275A/E	Rev.	1.00
Title	Notes on the Selection of the Clock Sources for RSCI8 and RSCI9 in the RX26T Group		Information Category	Technical Notification		
Applicable Product	RX26T Group	Lot No. All	Reference Document	RX26T Group User's Manual: Hardware Rev.1.10 (R01UH0979EJ0110)		

This document describes notes on the clock sources for the on-chip baud rate generators for channels 8 and 9 and for the Break Field transmission and detection timers for channel 9 in the serial communications interface (RSCI) of the RX26T group products.

1. Note

The baud rate generator only runs properly when the SCR2.CKS[1:0] bits in RSCI8 and RSCI9 are set to 00b. The Break Field transmission and detection timers only run properly when the XCR0.TCSS[1:0] bits in RSCI9 are set to 00b. RSCI11 does not have similar restrictions.

2. Workaround

The RSCI8.SCR2.CKS[1:0], RSCI9.SCR2.CKS[1:0], and RSCI9.XCR0.TCSS[1:0] bits should always be set to 00b.

3. Changes to the User's Manual

The following changes will be made to the user's manual: hardware regarding this issue.

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A footnote is added to the CKS[1:0] bits in section 33.2.7, Control Register 2 (SCR2) as follows.

Before change

Bit	Symbol	Bit Name	Description	R/W
			(Omitted)	
b21, b20	CKS[1:0]	Clock Select	b21 b20 0 0: PCLK (n = 0)*3 0 1: PCLK/4 (n = 1)*3 1 0: PCLK/16 (n = 2)*3 1 1: PCLK/64 (n = 3)*3	R/W *1
			(Omitted)	

Note 1. Writable only when SCR0.TE bit = 0 and SCR0.RE bit = 0.
Note 2. S is the value of S in BRR[7:0] bits explanation.
Note 3. n is the decimal notation of the value of n in BRR[7:0] bits explanation.

After change

Bit	Symbol	Bit Name	Description	R/W
			(Omitted)	
b21, b20	CKS[1:0]	Clock Select	b21 b20 0 0: PCLK (n = 0)*3 0 1: PCLK/4 (n = 1)*3, *4 1 0: PCLK/16 (n = 2)*3, *4 1 1: PCLK/64 (n = 3)*3, *4	R/W *1
			(Omitted)	

Note 1. Writable only when SCR0.TE bit = 0 and SCR0.RE bit = 0.
Note 2. S is the value of S in BRR[7:0] bits explanation.
Note 3. n is the decimal notation of the value of n in BRR[7:0] bits explanation.
Note 4. This setting is prohibited in RSCI8 and RSCI9.

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A footnote is added to Table 33.12, Clock Source Settings as follows.

Before change

Table 33.12 Clock Source Settings

SCR2 Setting		
CKS[1:0] Bits	**Clock Source**	**n**
0 0	PCLK	0
0 1	PCLK/4	1
1 0	PCLK/16	2
1 1	PCLK/64	3

After change

Table 33.12 Clock Source Settings

SCR2 Setting		
CKS[1:0] Bits	**Clock Source**	**n**
0 0	PCLK	0
0 1*1	PCLK/4	1
1 0*1	PCLK/16	2
1 1*1	PCLK/64	3

Note 1. This setting is prohibited in RSCI8 and RSCI9.

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A footnote is added to the TCSS[1:0] bits in section 33.2.14, Extended Serial Mode Control Register 0 (XCR0) as follows.

Before change

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TCSS[1:0]	Timer Count Clock Source Select	(Valid in extended serial mode) Select the clock source of the timer in the extended serial module. b1 b0 0 0: PCLK 0 1: PCLK/4 1 0: PCLK/16 1 1: PCLK/64	R/W *1,*2
(Omitted)				

Note 1. Writable only when SCR0.TE bit = 0 and SCR0.RE bit = 0.
Note 2. Rewrite the TCSS[1:0] bits only when the timer is stopped (XCR1.TCST bit = 0, XCR1.SDST bit = 0, and XCR1.BRME bit = 0).
Note 3. Base clock: 1/16 period of 1 bit period when SCR2.ABCS bit = 0, 1/8 period of 1 bit period when SCR2.ABCS bit = 1.
Note 4. This bit is a setting bit required for Start Frame reception operation. Rewrite this bit when Start Frame reception or transmission is not in progress (XCR1.SDST bit = 0 and XCR1.TCST bit = 0).

After change

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TCSS[1:0]	Timer Count Clock Source Select	(Valid in extended serial mode) Select the clock source of the timer in the extended serial module. b1 b0 0 0: PCLK 0 1: PCLK/4*5 1 0: PCLK/16*5 1 1: PCLK/64*5	R/W *1,*2
(Omitted)				

Note 1. Writable only when SCR0.TE bit = 0 and SCR0.RE bit = 0.
Note 2. Rewrite the TCSS[1:0] bits only when the timer is stopped (XCR1.TCST bit = 0, XCR1.SDST bit = 0, and XCR1.BRME bit = 0).
Note 3. Base clock: 1/16 period of 1 bit period when SCR2.ABCS bit = 0, 1/8 period of 1 bit period when SCR2.ABCS bit = 1.
Note 4. This bit is a setting bit required for Start Frame reception operation. Rewrite this bit when Start Frame reception or transmission is not in progress (XCR1.SDST bit = 0 and XCR1.TCST bit = 0).
Note 5. This setting is prohibited in RSCI9.