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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-R8C-A041A/E	Rev.	1.00
Title	Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt Revision of contents		Information Category	Technical Notification		
Applicable Product	R8C/5x Series R8C/Mx Series R8C/36T-A, R8C/38T-A Group	Lot No.	Reference Document	User's Manuals: Hardware of Applicable Products		

This document describes corrections to chapters "Voltage Monitor 1 Interrupt" and "Voltage Monitor 2 Interrupt" in the User's Manuals: Hardware of applicable products listed above.

Page and section numbers are based on the R8C/54E, R8C/54F, R8C/54G, R8C/54H Group User's Manual: Hardware Rev. 2.00 (R01UH0189EJ0200). For other product groups, refer to the corresponding pages.

Corrections

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Table 7.3 “Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt” is corrected as follows.

Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Before (the latest User’s Manual, Rev.2.00)

Step	When Digital Filter is Used	When Digital Filter is Not Used
1	Set bits VD1S0 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td (E-A).	
4	Set the IRQ1SEL bit in the CMPA register to select the interrupt type.	
5	Set bits VW1F0 and VW1F1 in the VW1C register to select the sampling clock for the digital filter.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
6(1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	-
7	Set the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register to select the timing for an interrupt request.	
8	Set the VW1C2 bit in the VW1C register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	-
10	Wait for 2 cycles of the sampling clock of the digital filter.	- (No wait time)
11(2)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled).	

Notes:
1. When the VW1C0 bit is 0, steps 5 and 6 can be performed at the same time (with one instruction).
2. When this setting is made with the voltage monitor 1 interrupt disabled (the VW1C0 bit is 0, the VCA26 bit is 0),
if VCC<Vdet1 (or VCC > Vdet1) is detected, no interrupt is generated until the voltage monitor 1 interrupt in step 11 is enabled. If VCC<Vdet1 (or VCC > Vdet1) is detected between steps 9 and 11, the VW1C2 bit is set to 1. Read the VW1C2 bit after step 11, and perform the processing required for detection if the read value is 1.

After

Step	When Digital Filter is Used	When Digital Filter is Not Used
1	Set bits VD1S0 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td (E-A).	
4	Set the IRQ1SEL bit in the CMPA register to select the interrupt type.	
5 (1)	Set bits VW1F0 and VW1F1 in the VW1C register to select the sampling clock for the digital filter.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
6 (1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	-
7 (1)	Set the VW1C7 bit in the VW1C register to select the timing for interrupt detection.	
8	Set the VCAC1 bit in the VCAC register to select the timing for interrupt detection.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	-
10	Wait for 4 cycles of the sampling clock (2 cycles of the low-speed on-chip oscillator clock) of the digital filter.	- (No wait time)
11	Set the VW1C2 bit in the VW1C register to 0.	
12 (2)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled).	

Notes:
1. When the VW1C0 bit is 0, steps 5 to 7 can be performed at the same time (with one instruction).
2. When this setting is made with the voltage monitor 1 interrupt disabled (the VW1C0 bit is 0, the VCA26 bit is 0),
if VCC<Vdet1 (or VCC > Vdet1) is detected, no interrupt is generated until the voltage monitor 1 interrupt in step 12 is enabled. If VCC<Vdet1 (or VCC > Vdet1) is detected between steps 11 and 12, the VW1C2 bit is set to 1. Read the VW1C2 bit after step 12, and perform the processing required for detection if the read value is 1.

Corrections

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Table 7.4 “Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt” is corrected as follows.

Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Before (the latest User’s Manual, Rev.2.00)

Step	When Digital Filter is Used	When Digital Filter is Not Used
1	Set the VCA23 bit in the VCA2 register to 0 (internal reference voltage).	
2 (1)	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
3	Wait for td (E-A).	
4	Set the IRQ2SEL bit in the CMPA register to select the interrupt type.	
5	Set bits VW2F0 and VW2F1 in the VW2C register to select the sampling clock for the digital filter.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
6 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	-
7	Set the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register to select the timing for an interrupt request.	
8	Set the VW2C bit in the VW2C2 register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	-
10	Wait for 2 cycles of the sampling clock of the digital filter.	- (No wait time)
11 (3)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is 0, steps 1 and 2 can be performed at the same time (with one instruction).
2. When the VW2C0 bit is 0, steps 5 and 6 can be performed at the same time (with one instruction).
3. When this setting is made with the voltage monitor 2 interrupt disabled (the VW2C0 bit is 0, the VCA27 bit is 0), if VCC<Vdet2 (or VCC > Vdet2) is detected, no interrupt is generated until the voltage monitor 2 interrupt in step 11 is enabled. If VCC<Vdet2 (or VCC > Vdet2) is detected between steps 9 and 11, the VW2C2 bit is set to 1. Read the VW2C2 bit after step 11, and perform the processing required for detection if the read value is 1.

After

Step	When Digital Filter is Used	When Digital Filter is Not Used
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td (E-A).	
3	Set the IRQ2SEL bit in the CMPA register to select the interrupt type.	
4 (1)	Set bits VW2F0 and VW2F1 in the VW2C register to select the sampling clock for the digital filter.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
5 (1)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	-
6 (1)	Set the VW2C7 bit in the VW2C register to select the timing for interrupt detection.	
7	Set the VCAC2 bit in the VCAC register to select the timing for interrupt detection.	
8	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	-
9	Wait for 4 cycles of the sampling clock (2 cycles of the low-speed on-chip oscillator clock) of the digital filter.	- (No wait time)
10	Set the VW2C2 bit in the VW2C register to 0.	
11 (2)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is 0, steps 4 to 6 can be performed at the same time (with one instruction).
2. When this setting is made with the voltage monitor 2 interrupt disabled (the VW2C0 bit is 0, the VCA27 bit is 0), if VCC<Vdet2 (or VCC > Vdet2) is detected, no interrupt is generated until the voltage monitor 2 interrupt in step 11 is enabled. If VCC<Vdet2 (or VCC > Vdet2) is detected between steps 10 and 11, the VW2C2 bit is set to 1. Read the VW2C2 bit after step 11, and perform the processing required for detection if the read value is 1.