

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A164A/E	Rev.	1.00
Title	R8C/Tiny Series Notes on Writing to Timer RA Register		Information Category	Technical Notification		
Applicable Product	See Below	Lot No.	Reference Document			
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1. Usage Notes

In all timer RA modes, if writing is performed to the applicable registers below during counting operation (TCSTF bit is set to 1), writing to the same register is not accepted for a certain period.

Applicable registers: Timer RA prescaler register (TRAPRE register), timer RA register (TRA register)

1) TRAPRE register

If the TRAPRE register is written during count operation (TCSTF bit is set to 1) and when the prescaler value shown in Figure 1 is any N (period A), writing to the TRAPRE register is not accepted when the consecutive prescaler value is N-1 (period B).

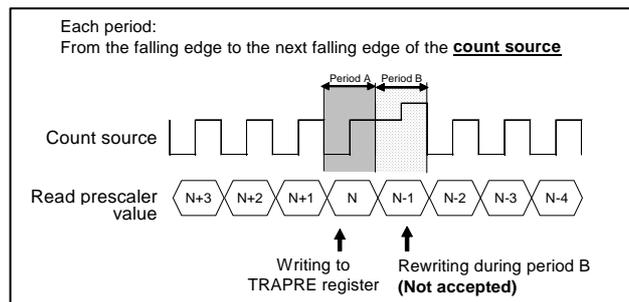


Figure 1 Continuous Writing to TRAPRE Register

2) TRA register

i) In timer mode, pulse output mode, event counter mode, and pulse period measurement mode

If the TRA register is written during count operation (TCSTF bit is set to 1) and when the counter value shown in Figure 2 is any N (period C), writing to the TRA register is not accepted when the consecutive counter value is N-1 (period D).

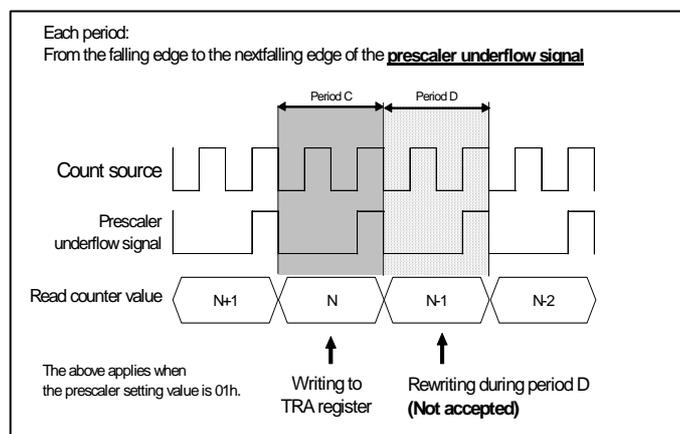


Figure 2 Continuous Writing to TRA Register in Timer Mode, Pulse Output Mode, Event Counter Mode, and Pulse Period Measurement Mode

ii) In pulse period measurement mode

During count operation (TCSTF bit is set to 1) and during pulse width measurement (a measurement pulse is input to the INT1/TRAI0 pin), if the TRA register is written when the counter value shown in Figure 3 is any N (interval E'), writing to the TRA register is not accepted when the consecutive counter value is N-1 (interval F').

During count operation (TCSTF bit is set to 1) and when the pulse width is not measured (no measurement pulse is input to the INT1/TRAI0 pin), if TRA register is written during interval E in Figure 3, writing to the TRA register is not accepted during consecutive interval F.

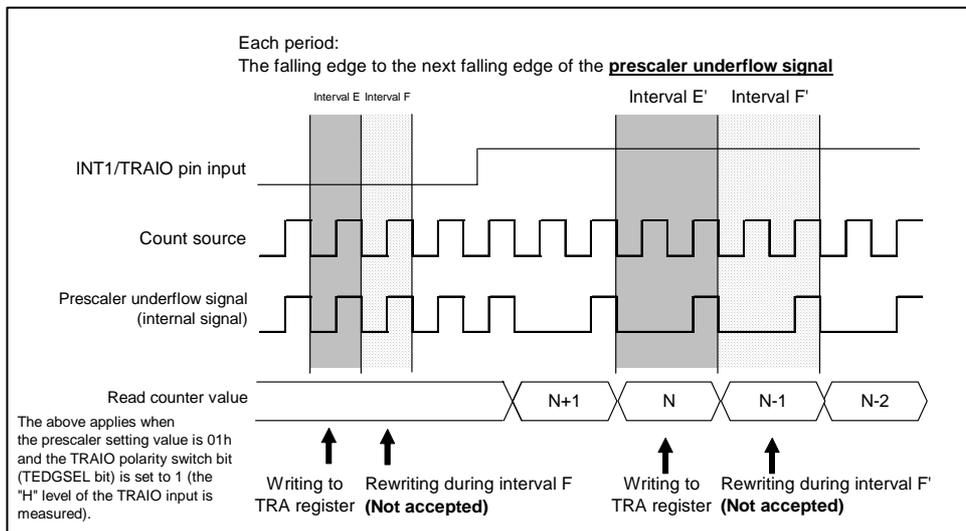


Figure 3 Continuous Writing to TRA Register in Pulse Width Measurement Mode

2. Countermeasures

1) TRAPRE register

When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.

2) TRA register

When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

3. Applicable Products

R8C/20 Group, R8C/21 Group, R8C/22 Group, R8C/23 Group, R8C/24 Group, R8C/25 Group, R8C/26 Group, R8C/27 Group, R8C/28 Group, R8C/29 Group, R8C/2A Group, R8C/2B Group, R8C/2C Group, R8C/2D Group