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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0072A/E	Rev.	1.00
Title	RA4E1 Group, RA4M2 Group, RA4M3 Group, RA6E1 Group, RA6M4 Group, RA6M5 Group, correction of Quad Serial Peripheral Interface (QSPI)		Information Category	Technical Notification		
Applicable Product	RA4E1 Group RA4M2 Group RA4M3 Group RA6E1 Group RA6M4 Group RA6M5 Group	Lot No. All	Reference Document	RA4E1 Group User's Manual Hardware Rev.1.10 RA4M2 Group User's Manual Hardware Rev.1.10 RA4M3 Group User's Manual Hardware Rev.1.30 RA6E1 Group User's Manual Hardware Rev.1.10 RA6M4 Group User's Manual Hardware Rev.1.20 RA6M5 Group User's Manual Hardware Rev.1.20		

The descriptions of Quad Serial Peripheral Interface (QSPI) are corrected.

1.External Bus Space

RA4E1 Page 1139, RA4M2 Page 1202, RA4M3 Page 1215, RA6E1 Page 1256, RA6M4 Page 1333, RA6M5 Page 1643

[Before]

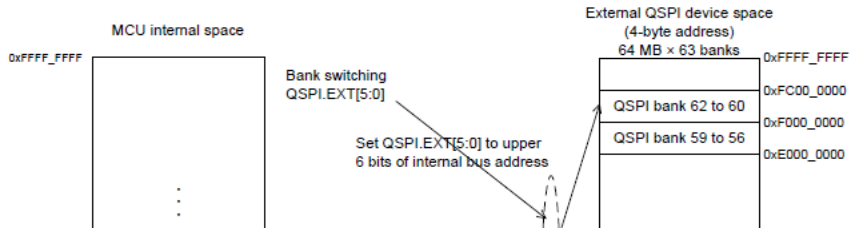

Figure Default- area setting and memory map

[After]

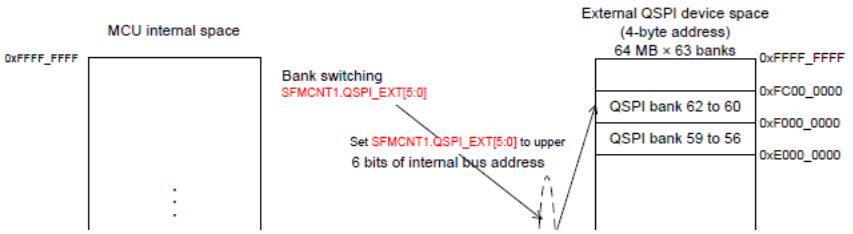

Figure Default- area setting and memory map

2. Hold Time for Serial Data Output

RA4E1 Page 1148, RA4M2 Page 1211, RA4M3 Page 1224, RA6E1 Page 1265, RA6M4 Page 1342, RA6M5 Page 1652

[Before]

When a command or address is transmitted to the serial flash memory, the hold time begins on the rising edge of QSPCLK and ends when the serial data makes another transmission. If this hold time is insufficient, it can be extended by 1 PCLKA using the SFMOHW bit in the SFMSMD register. When SFMOSW is 1, the high-level width of QSPCLK during serial data transmission is extended by 1 PCLKA while data is being output from the QSPI. This function has no effect on serial data reception.

[After]

When a command or address is transmitted to the serial flash memory, the hold time begins on the rising edge of QSPCLK and ends when the serial data makes another transmission. If this hold time is insufficient, it can be extended by 1 PCLKA using the SFMOHW bit in the SFMSMD register. When SFMOHW is 1, the high-level width of QSPCLK during serial data transmission is extended by 1 PCLKA while data is being output from the QSPI. This function has no effect on serial data reception.

3. Fast Read Quad Output Instruction

RA4E1 Page 1154, RA4M2 Page 1218, RA4M3 Page 1230, RA6E1 Page 1271, RA6M4 Page 1348, RA6M5 Page 1658

[Before]

The Fast Read Quad Output instruction is a read instruction that uses four signal lines to receive data. When the SPI bus cycle starts, the QSSL signal is asserted. The instruction code (0x6B or 0x6C) and an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, are output from the QIO0 pin. Next, a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSMD register, are generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

[After]

The Fast Read Quad Output instruction is a read instruction that uses four signal lines to receive data. When the SPI bus cycle starts, the QSSL signal is asserted. The instruction code (0x6B or 0x6C) and an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, are output from the QIO0 pin. Next, a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSDC register, are generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

4. Fast Read Quad I/O Instruction

RA4E1 Page 1155, RA4M2 Page 1219, RA4M3 Page 1231, RA6E1 Page 1272, RA6M4 Page 1349, RA6M5 Page 1659

[Before]

The Fast Read Quad I/O instruction is a read instruction that uses four signal lines to transmit an address and receive data. When the SPI bus cycle starts, the QSSL signal is asserted, and the instruction code (0xEB / 0xEC) is transmitted from QIO0 pin in the extended SPI protocol and from QIO0, QIO1, QIO2, and QIO3 pins in the Quad-SPI protocol. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted through the QIO0, QIO1, QIO2, and QIO3 pins, and a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSMD register, is generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

[After]

The Fast Read Quad I/O instruction is a read instruction that uses four signal lines to transmit an address and receive data. When the SPI bus cycle starts, the QSSL signal is asserted, and the instruction code (0xEB / 0xEC) is transmitted from QIO0 pin in the extended SPI protocol and from QIO0, QIO1, QIO2, and QIO3 pins in the Quad-SPI protocol. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted through the QIO0, QIO1, QIO2, and QIO3 pins, and a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSDC register, is generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.