

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0073B/E	Rev.	2.00
Title	RA4M2 Group, RA4M3 Group, RA6E1 Group, RA6M4 Group, RA6M5 Group, correction of Serial Sound Interface Enhanced (SSIE)		Information Category	Technical Notification		
Applicable Product	RA4M2 Group RA4M3 Group RA6E1 Group RA6M4 Group RA6M5 Group	Lot No. All	Reference Document	RA4M2 Group User's Manual Hardware Rev.1.10 RA4M3 Group User's Manual Hardware Rev.1.30 RA6E1 Group User's Manual Hardware Rev.1.10 RA6M4 Group User's Manual Hardware Rev.1.20 RA6M5 Group User's Manual Hardware Rev.1.20		

The descriptions of Serial Sound Interface Enhanced (SSIE) are corrected.

1.SSIFCR : FIFO Control Register

RA4M2 Page 1263, RA4M3 Page 1276, RA6E1 Page 1317, RA6M4 Page 1438, RA6M5 Page 1803

[Before]

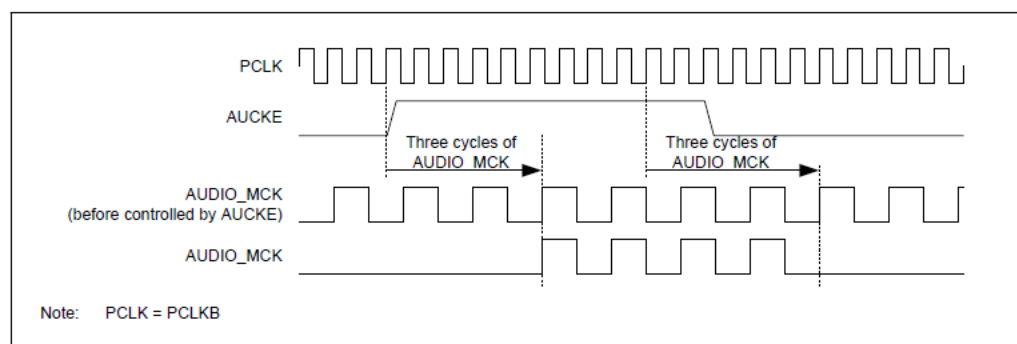


Figure Stop/resume of AUDIO_MCK

[After]

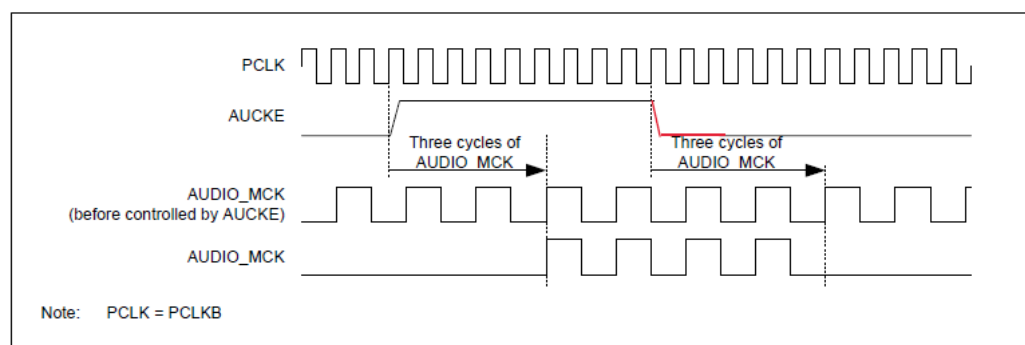


Figure Stop/resume of AUDIO_MCK

2.SSIFSR : FIFO Status Register

RA4M2 Page 1264, RA4M3 Page 1277, RA6E1 Page 1318, RA6M4 Page 1439, RA6M5 Page 1804

[Before]

Bit	Symbol	Function	R/W
13:8	RDC[5:0]	Number of Receive FIFO Data Indication Flag Number of receive FIFO data indication flag	R
29:24	TDC[5:0]	Number of Transmit FIFO Data Indication Flag Number of transmit FIFO data indication flag	R

RDC[5:0] flags (Number of Receive FIFO Data Indication Flag)

The RDC[5:0] flags indicate the number of valid data that are stored in the receive FIFO data register (SSIFRDR). With this flag as 0x00, there is no received data. With 0x20, the register is filled with received data and there is no free space.

TDC[5:0] flags (Number of Transmit FIFO Data Indication Flag)

The TDC[5:0] flags indicate the number of valid data that are stored in the transmit FIFO data register (SSIFTDR). With this flag as 0x00, there is no data to be transmitted. With 0x20, there is no space to write data.

[After]

Bit	Symbol	Function	R/W
13:8	RDC[5:0]	Receive Data Count Number of valid data stored in the receive FIFO data register	R
29:24	TDC[5:0]	Transmit Data Count Number of valid data stored in the transmit FIFO data register	R

RDC[5:0] bits (Receive Data Count)

The RDC[5:0] bits indicate the number of valid data that are stored in the receive FIFO data register (SSIFRDR). With these bits as 0x00, there is no received data. With 0x20, the register is filled with received data and there is no free space.

TDC[5:0] bits (Transmit Data Count)

The TDC[5:0] bits indicate the number of valid data that are stored in the transmit FIFO data register (SSIFTDR). With these bits as 0x00, there is no data to be transmitted. With 0x20, there is no space to write data.

3.SSIFTDR : Transmit FIFO Data Register

RA4M2 Page 1269, RA4M3 Page 1282, RA6E1 Page 1323, RA6M4 Page 1444, RA6M5 Page 1809

[Before]

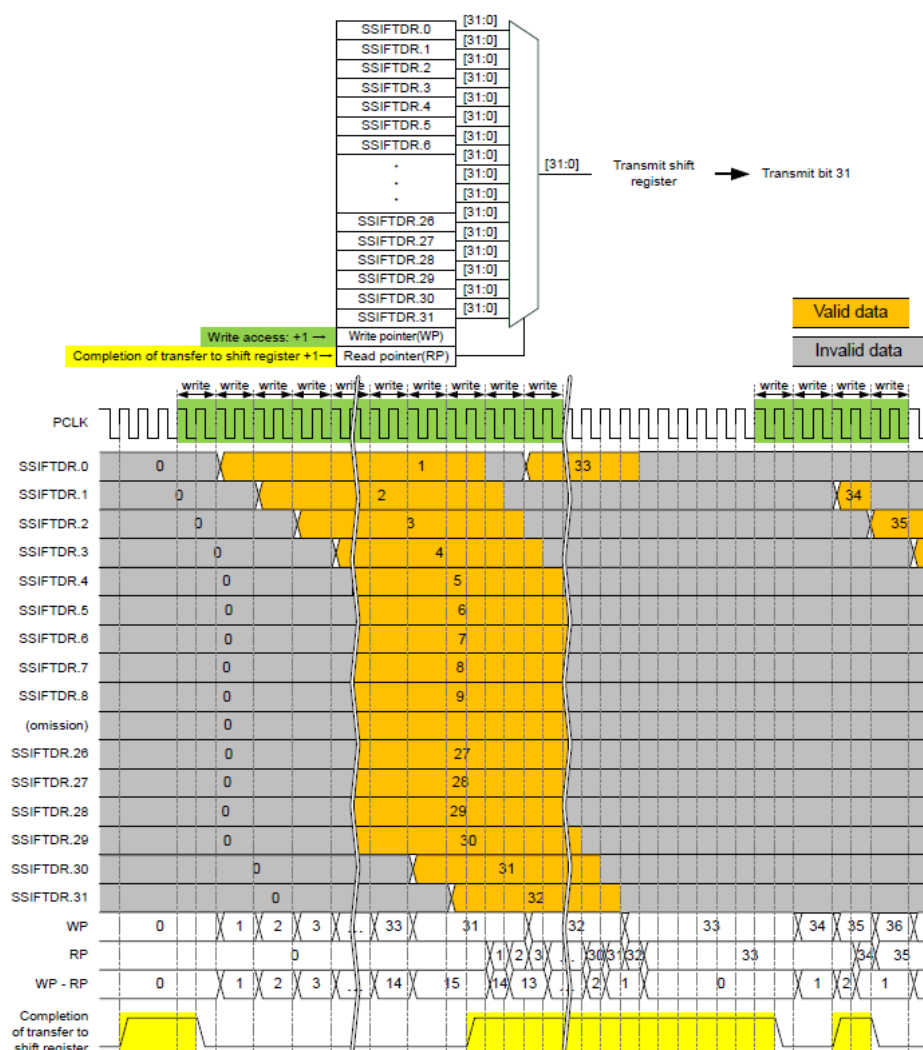


Figure Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example

[After]

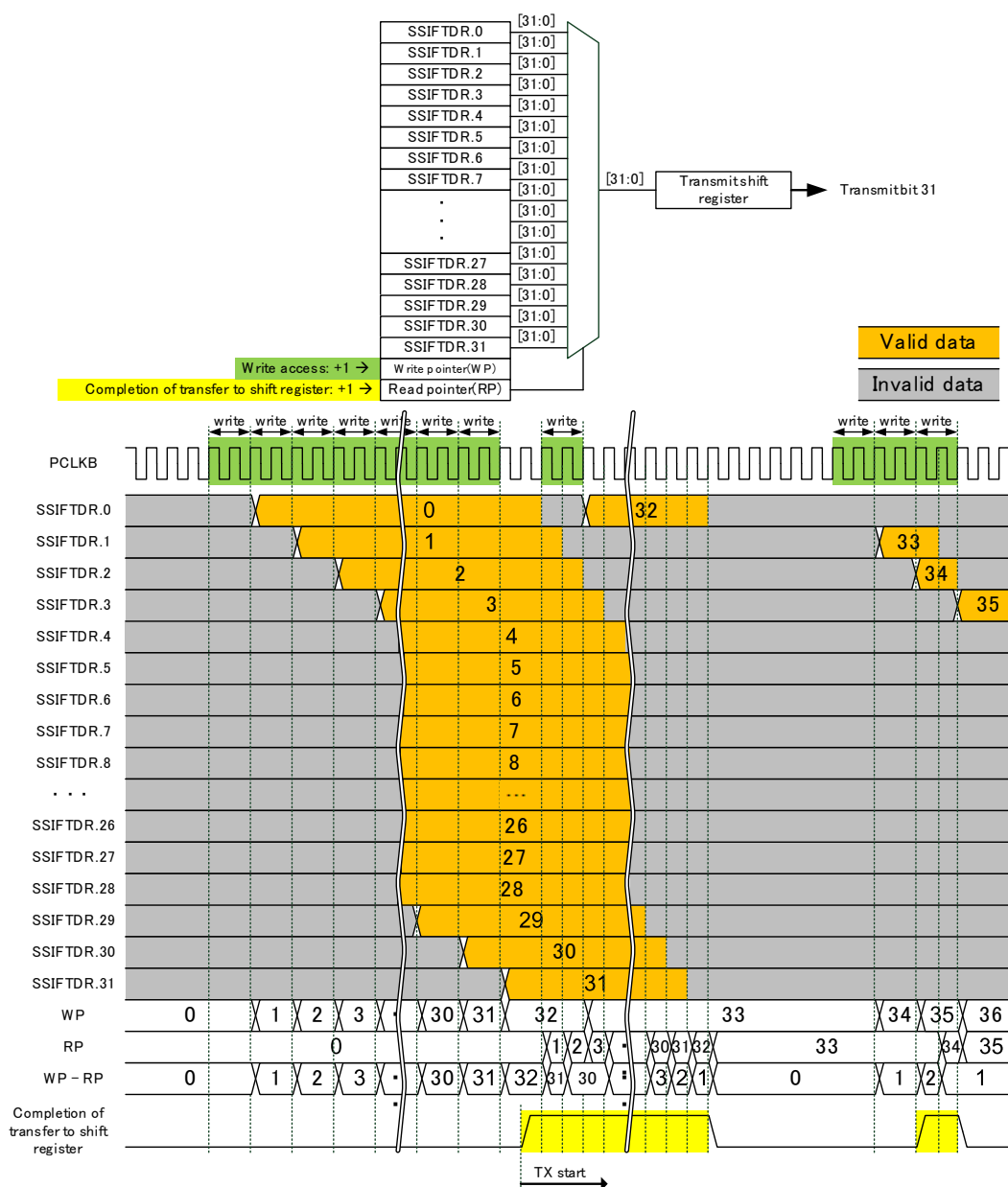


Figure Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example

4.SSIFRDR : Receive FIFO Data Register

RA4M2 Page 1270, RA4M3 Page 1283, RA6E1 Page 1324, RA6M4 Page 1445, RA6M5 Page 1810

[Before] example: RA6M4

Figure 35.31 shows the configurations and operation examples of the receive FIFO data register and receive shift register.

[After]

Figure 35.32 shows the configurations and operation examples of the receive FIFO data register and receive shift register.

5.SSIFRDR : Receive FIFO Data Register

RA4M2 Page 1271, RA4M3 Page 1284, RA6E1 Page 1325, RA6M4 Page 1446, RA6M5 Page 1811

[Before]

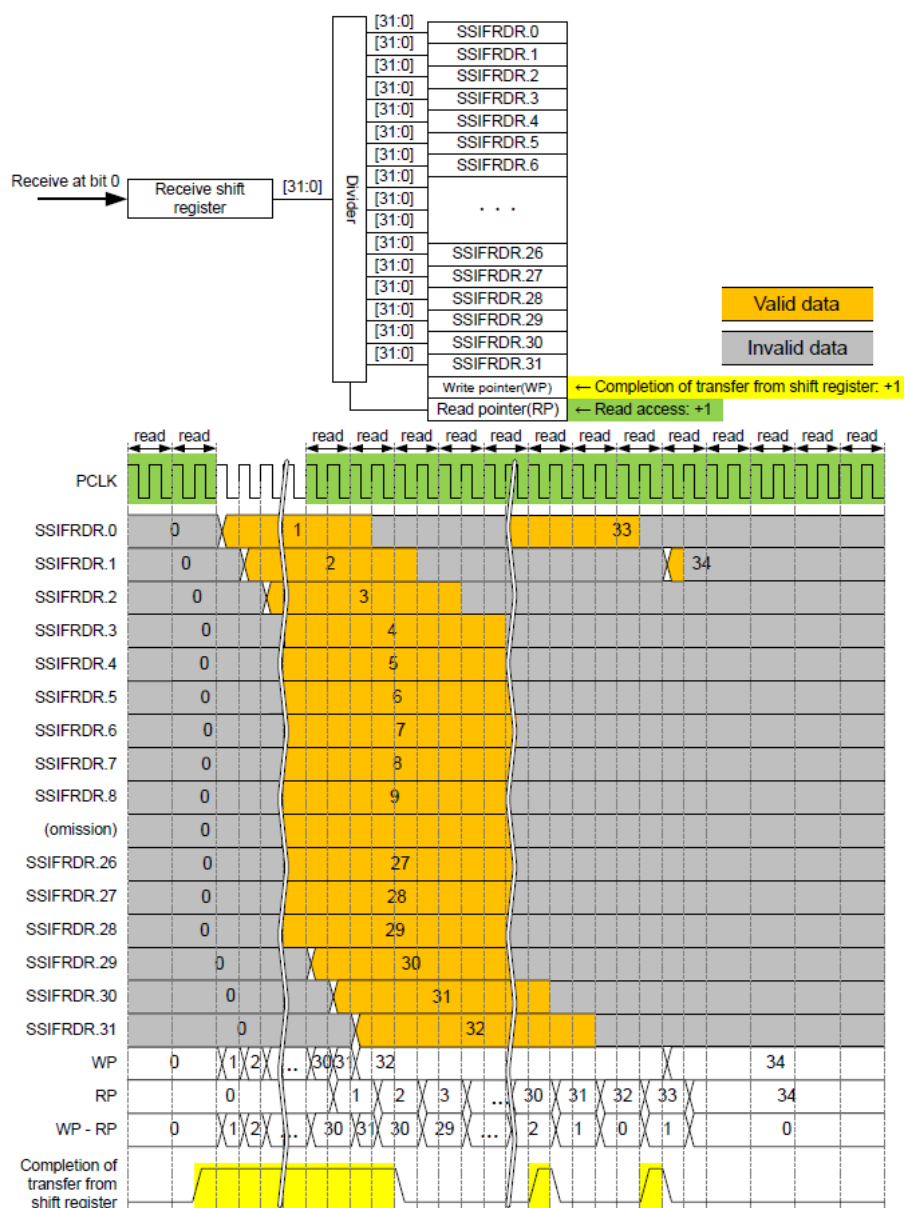


Figure Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example

[After]

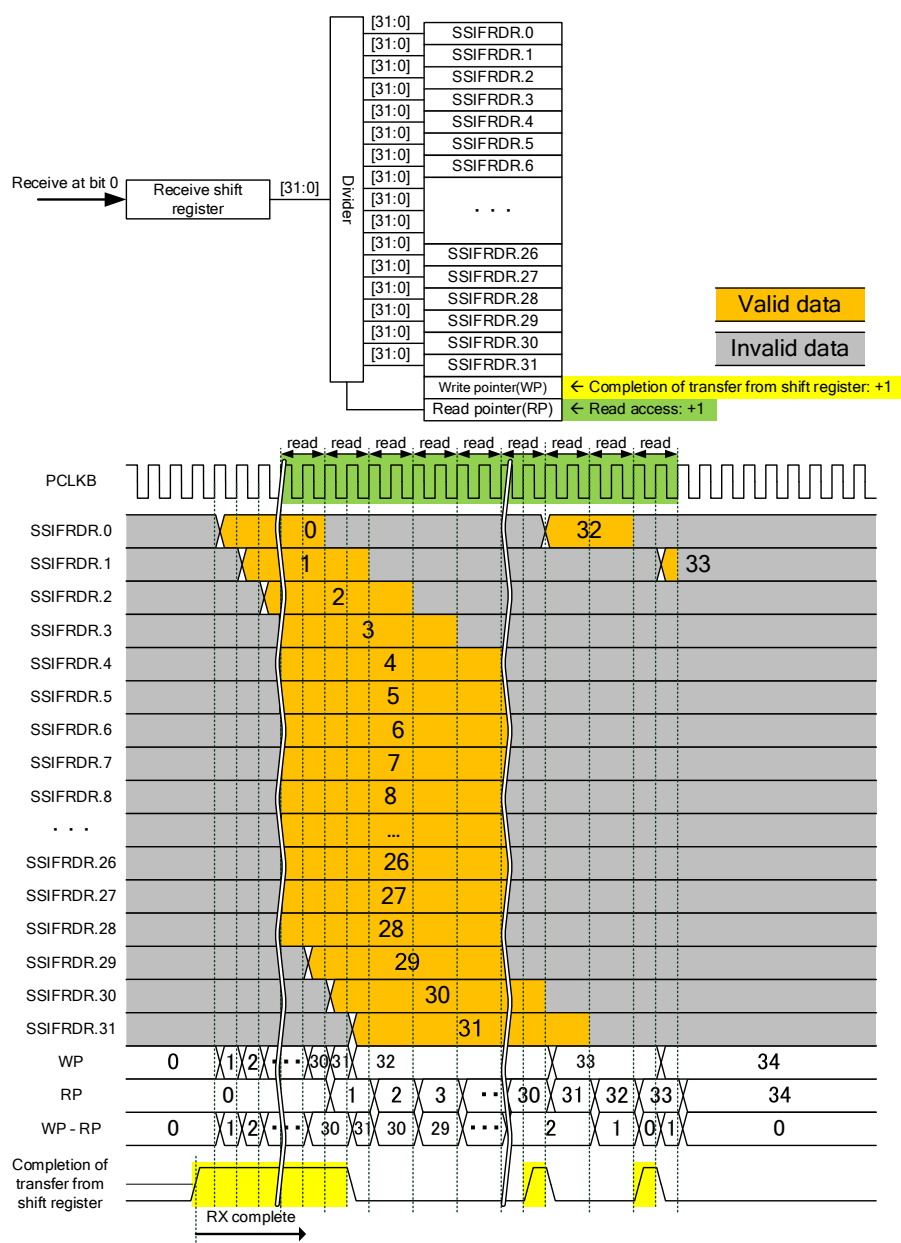


Figure Configuration of the **receive** FIFO data register and **receive** shift register, and FIFO operation example

6.Data communication state

RA4M2 Page 1285, RA4M3 Page 1298, RA6E1 Page 1339, RA6M4 Page 1460, RA6M5 Page 1825

[Before] example: RA6M4

- State Transition in the Setting with Padding Bits

When SSIE ends transfer of the last bit of a data word during communication (SSISR.IIRQ = 0), SSIE transitions from the data communication state to the padding communication state in Figure 35.49. Except in the status with SSICR.SDTA = 1 and transmission and reception disabled (SSICR.TEN = 0 and SSICR.REN = 0), SSIE transitions from the data communication state to the idle state when it stops communication in Figure 35.51.

[After]

- State Transition in the Setting with Padding Bits

When SSIE ends transfer of the last bit of a data word during communication (SSISR.IIRQ = 0), SSIE transitions from the data communication state to the padding communication state in Figure 35.49. Except in the status with SSICR.SDTA = 1 and transmission and reception disabled (SSICR.TEN = 0 and SSICR.REN = 0), SSIE transitions from the data communication state to the idle state when it stops communication in **Figure 35.50**.