RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RH8-B0493B/E	Rev.	2.00
Title	RH850/P1x-C, P1L-C GTM limitations		Information Category	Technical Notification		
Applicable Product	RH850/P1H-C, RH850/P1M-C, RH850/P1L-C	Lot No.	Reference Document	・RH850/P1x-C Group User's Manual: Hardware, R01UH0517EJ0140 ・RH850/P1L-C Group User's Manual: Hardware, R01UH0592EJ0120		
		All lot				

This document describes the GTM limitation which will be added to above Reference Document.

For RH850/P1H-C and RH850/P1M-C, following descriptions will be added to section 25.20 CAUTION as ID37.

For RH850/P1L-C, following descriptions will be added to section 21.20 CAUTION as ID37.

Title

   ID37: ATOM: Missing edge on output signal ATOM_OUT

Effects:

   Missing edge on output signal ATOM_OUT.

Description (**update**)

   If an ATOM channel is configured to be triggered by a previous channel by setting of GTM0ATOMixCTRL.RST_CCU0=1 (SOMP mode in ATOM) and there is a pipeline**/synchronization** register within the trigger chain between the triggering channel and the triggered channel, the edge to the inverse SL at the output signal ATOM_OUT is not generated for GTM0ATOMixCM1.CM1=1 and GTM0ATOMixCM0.CM0>1. **The problem only occurs if the selected clock resolution for the triggered channel has a divider factor of more than 1 related to the GTM global clock SYS_CLK.**

Workaround

   Workaround 1: (**update**)

   If available use channels without a pipeline**/synchronization** register within the trigger chain between the triggering channel and the triggered channel.

   Workaround 2:

   Switch the order of the edges, so that GTM0ATOMixCM0.CM0 defines the first edge and GTM0ATOMixCM1.CM1 the second edge. Additionally invert the SL value to get the same waveform on the output signal ATOM_OUT.

   Note: In this case, to generate 0% duty cycle, don't use GTM0ATOMixCM1.CM1=GTM0ATOMixCM0.CM0.Instead, use GTM0ATOMixCM1.CM1=1 and GTM0ATOMixCM0.CM0=MAX. However, this only works in the non-fixed (relevant) releases.

   Workaround 3:

   Use a clock resolution for the triggered channel with a divider value of 1 related to the cluster clock.