Date: Jan. 19, 2023

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0107A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1D Descriptions in the User's Manual: Hardware Rev. 1.30 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1D Group	Lot No. All lots	Reference Document	RL78/G1D User's Manual: Hardware Rev. 1.30 R01UH0515EJ0130 (Mar. 2018)		

This document describes misstatements found in the RL78/G1D User's Manual: Hardware Rev. 1.30 (R01UH0515EJ0130).

Corrections

Applicable Item	Applicable Page	Contents
8.3.4 Real-time clock control register 1 (RTCC1)	Page 271	Incorrect descriptions revised
Figure 8-21. Procedure for Reading Real-time Clock	Page 284	Incorrect descriptions revised
Figure 8-22. Procedure for Writing Real-time Clock	Page 285	Incorrect descriptions revised
30.5.1 MCU	Page 823 to Page 826	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0515EJ0130	
1	8.3.4 Real-time clock control register 1 (RTCC1)		Page 271	Page 3
2	Figure 8-21. Procedure for Reading Real-time Clock		Page 284	Page 4
3	Figure 8-22. Procedure for Writing Real-time Clock		Page 285	Page 4
4	30.5.1 MCU		Page 823 to Page 826	Page 5 to Page 7

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G1D Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0107A/E	Jan. 19, 2023	First edition issued Corrections No.1 to No.4 revised (this document)

1. 8.3.4 Real-time clock control register 1 (RTCC1) (Page 271)

Incorrect:

Figure 8-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1).Notes 1, 2 When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

Correct:

Figure 8-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt. When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1).Notes 1, 2 When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

2. Figure 8-21. Procedure for Reading Real-time Clock (Page 284)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

Correct:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

3. Figure 8-22. Procedure for Writing Real-time Clock (Page 285)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

Correct:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

4. 30.5.1 MCU (Page 823 to Page 826)

Incorrect:

30.5.1 MCU

(1) Operating current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Operating current Note 1	I_{DD1}	HS (high-speed main) mode Note 5	Basic operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		2.3		mA
			Normal operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		5.2	8.5	mA
					T_A = +85°C Note 6		5.7	13.3	µA
							5.8	13.4	µA

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

2. When high-speed system clock and subsystem clock are stopped.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). **Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

6. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Correct:

30.5.1 MCU

(1) Operating current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Operating current Note 1	I_{DD1}	HS (high-speed main) mode Note 5	Basic operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		2.3		mA
			Normal operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		5.2	8.5	mA
					T_A = +85°C Note 6		5.7	13.3	µA
							5.8	13.4	µA

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

2. When high-speed system clock and subsystem clock are stopped.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

6. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(2) Standby current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
HALT current Note 1, 2	I_{DD2}	HS (high-speed main) mode Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 3.0 V		0.62	1.86	mA
			f_{IH} = 24 MHz Note 4	V_{DD} = 3.0 V		0.50	1.45	mA
			f_{IH} = 16 MHz Note 4	V_{DD} = 3.0 V		0.44	1.11	mA
		LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		290	620	µA
				V_{DD} = 2.0 V		290	620	µA
		LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		440	680	µA
				V_{DD} = 2.0 V		440	680	µA
		HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 9		0.31	1.08	mA
						0.48	1.28	mA
			f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 9		0.21	0.63	mA
						0.28	0.71	mA
		LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 9		110	360	µA
						160	420	µA
				V_{DD} = 2.0 V Note 9		110	360	µA
						160	420	µA
		Subsystem clock operation	f_{SUB} = 32.768kHz Note 5	T_A = –40°C Note 9		0.28	0.61	µA
						0.47	0.80	µA
				T_A = +25°C Note 9		0.34	0.61	µA
						0.53	0.80	µA
				T_A = +50°C Note 9		0.41	2.30	µA
						0.60	2.49	µA
				T_A = +70°C Note 9		0.64	4.03	µA
						0.83	4.22	µA
				T_A = +85°C Note 9		1.09	8.04	µA
						1.28	8.23	µA
STOP current Note 6, 8	I_{DD3}	T_A = –40°C				0.19	0.52	µA
		T_A = +25°C				0.25	0.52	µA
		T_A = +50°C				0.32	2.21	µA
		T_A = +70°C				0.55	3.94	µA
		T_A = +85°C				1.00	7.95	µA

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

(2) Standby current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
HALT current Note 1, 2	I_{DD2}	HS (high-speed main) mode Note 6	f_{IH} = 32 MHz Note 4	V_{DD} = 3.0 V		0.62	1.86	mA
			f_{IH} = 24 MHz Note 4	V_{DD} = 3.0 V		0.50	1.45	mA
			f_{IH} = 16 MHz Note 4	V_{DD} = 3.0 V		0.44	1.11	mA
		LS (low-speed main) mode Note 6	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		290	620	µA
				V_{DD} = 2.0 V		290	620	µA
		LV (low-voltage main) mode Note 6	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		440	680	µA
				V_{DD} = 2.0 V		440	680	µA
		HS (high-speed main) mode Note 6	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 8		0.31	1.08	mA
						0.48	1.28	mA
			f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 8		0.21	0.63	mA
						0.28	0.71	mA
		LS (low-speed main) mode Note 6	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 8		110	360	µA
						160	420	µA
				V_{DD} = 2.0 V Note 8		110	360	µA
						160	420	µA
		Subsystem clock operation	f_{SUB} = 32.768kHz Note 5	T_A = –40°C Note 8		0.28	0.61	µA
						0.47	0.80	µA
				T_A = +25°C Note 8		0.34	0.61	µA
						0.53	0.80	µA
				T_A = +50°C Note 8		0.41	2.30	µA
						0.60	2.49	µA
				T_A = +70°C Note 8		0.64	4.03	µA
						0.83	4.22	µA
				T_A = +85°C Note 8		1.09	8.04	µA
						1.28	8.23	µA
STOP current Note 7	I_{DD3}	T_A = –40°C				0.19	0.52	µA
		T_A = +25°C				0.25	0.52	µA
		T_A = +50°C				0.32	2.21	µA
		T_A = +70°C				0.55	3.94	µA
		T_A = +85°C				1.00	7.95	µA

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
6. **Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
   2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
   LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
   LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz
8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
9. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1).
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
   2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
   LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
   LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz
7. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
8. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)
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3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C