

White Paper

Carrying the Heat Away from Power Module PCB Designs

Power system designers are always seeking higher power capability on smaller footprints. This is particularly true for datacenter servers and LTE base stations that support high current loads from increasingly power hungry FPGAs, ASICs and microprocessors. To reach higher output currents, multi-phase systems are being used more and more. To achieve higher current levels on smaller footprints, system designers are moving away from discrete power solutions in favor of power modules. That's because modules offer a popular alternative to complex power designs and the printed circuit board (PCB) layout issues associated with DC/DC converters.

This article discusses a multi-layer PCB layout method that uses via placements to maximize the thermal performance of a dual phase power module. The module features two single phase outputs at 20A each, or a dual phase single 40A output. An example board design with vias is used to illustrate higher power densities while carrying heat away from the power module, enabling operation without heat sinks or fans.

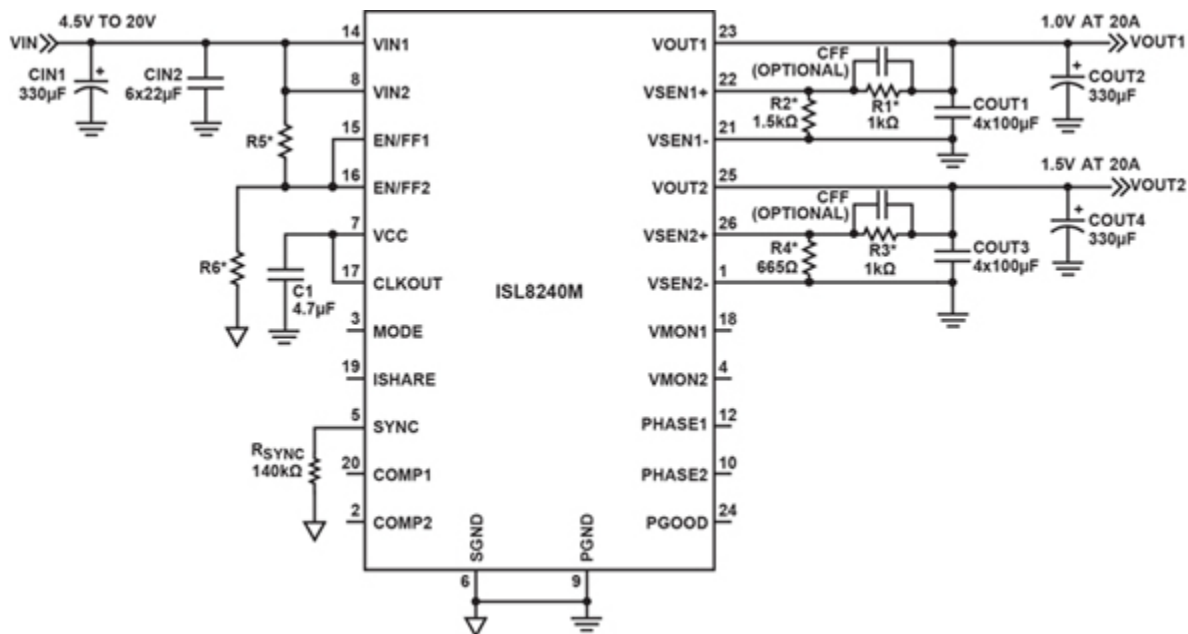


Figure 1. ISL8240M Circuit Showing Two Outputs That Can Source 20A Each

So how can this module achieve such high power density? The power module shown in the schematic in Figure 1 offers a very low thermal resistance specification θ_{JA} of only 8.5 °C/W because it uses copper as its substrate. To remove heat from the module, it is mounted on a highly effective thermal conductivity circuit board with direct attach features. This multi-layer circuit board has a top trace layer on which the module is mounted and two buried copper planes which are connected with vias to the top layer. This structure has very high thermal conductivity (low thermal resistance), which allows heat to readily flow away from the module.

To understand how this works, let's examine the ISL8240MEVAL4Z evaluation board implementation (Figure 2). The ISL8240MEVAL4Z is a four layer board that supports the step-down power module in its dual output mode sourcing 20A on each output.

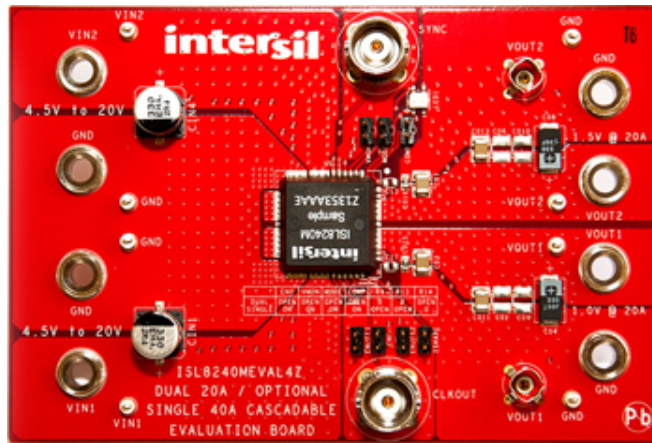


Figure 2. ISL8240MEVAL4Z Power Module Evaluation Board

The board uses four PCB layers with a nominal thickness of 0.062 inches ($\pm 10\%$), and has a stack arrangement as shown in Figure 3.

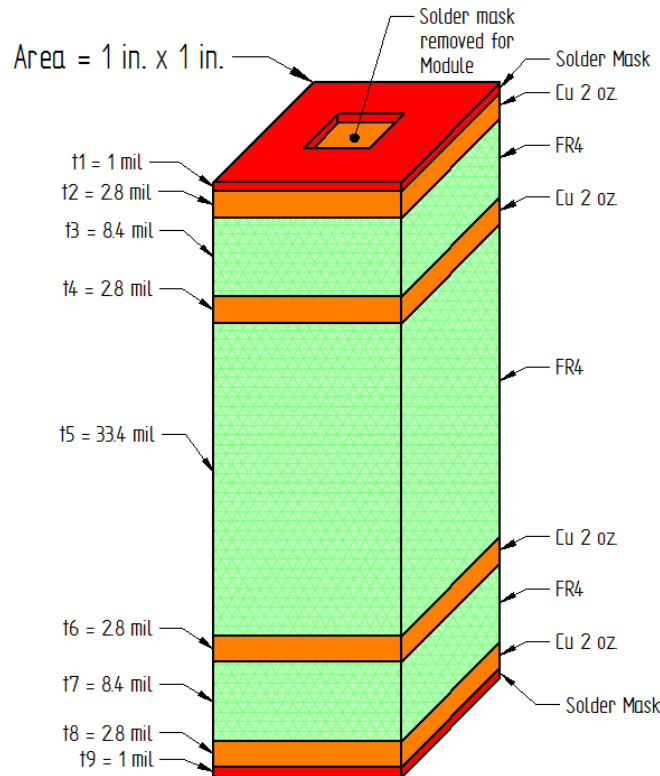


Figure 3. Stack Arrangement of Four Layer 0.062 Inch Board Used by ISL8240M Power Module

The PCB is composed primarily of FR4 circuit board material and copper with smaller amounts of solder, nickel and gold. Table 1 lists the thermal conductivity factors of the primary materials.

Table 1. Thermal Conductivity Factors for PCB Materials

Components	K(W/in-C)	K (W/m-K)
Air	0.0007	0.0275
Copper	9	355
FR4	0.0064	0.25
Solder Mask	0.0054	0.21
SAC305*	1.47	58

- SAC305* is the most popular lead-free solder composed of tin 96.5%, silver 3.0% and copper 0.5%
- W = watts; in = inches; C = degrees C; m = meters; K = degrees Kelvin

Equation 1 is used to determine the thermal resistance of a material.

$$\theta = \frac{t}{K \times A \times B}$$

Equation 1. Materials Thermal Resistance Calculation

To determine the thermal resistance of the board’s top copper layer in Figure 3, take the thickness of the copper layer (*t*) and divide it by the thermal conductivity factor multiplied by the cross sectional area. We have conveniently used 1 square inch with the dimensions *A* = *B* = 1 inch as the cross sectional area. The thickness of the copper layer is 2.8 mil or 0.0028 inches. This is the thickness of 2 oz. of copper deposited on one square foot of board area. The factor *K* is the W/(in-°C) factor for copper, which is nine. Therefore, the thermal resistance to heat flow of this one square inch of 2.8 mil copper is 0.0028/9 = 0.0003 °C/W. You can use the dimension shown in Figure 3 for each layer and the appropriate *K* factor from Table 1 to calculate the thermal resistance of each layer of the one square inch board area. The results are shown in Figure 4.

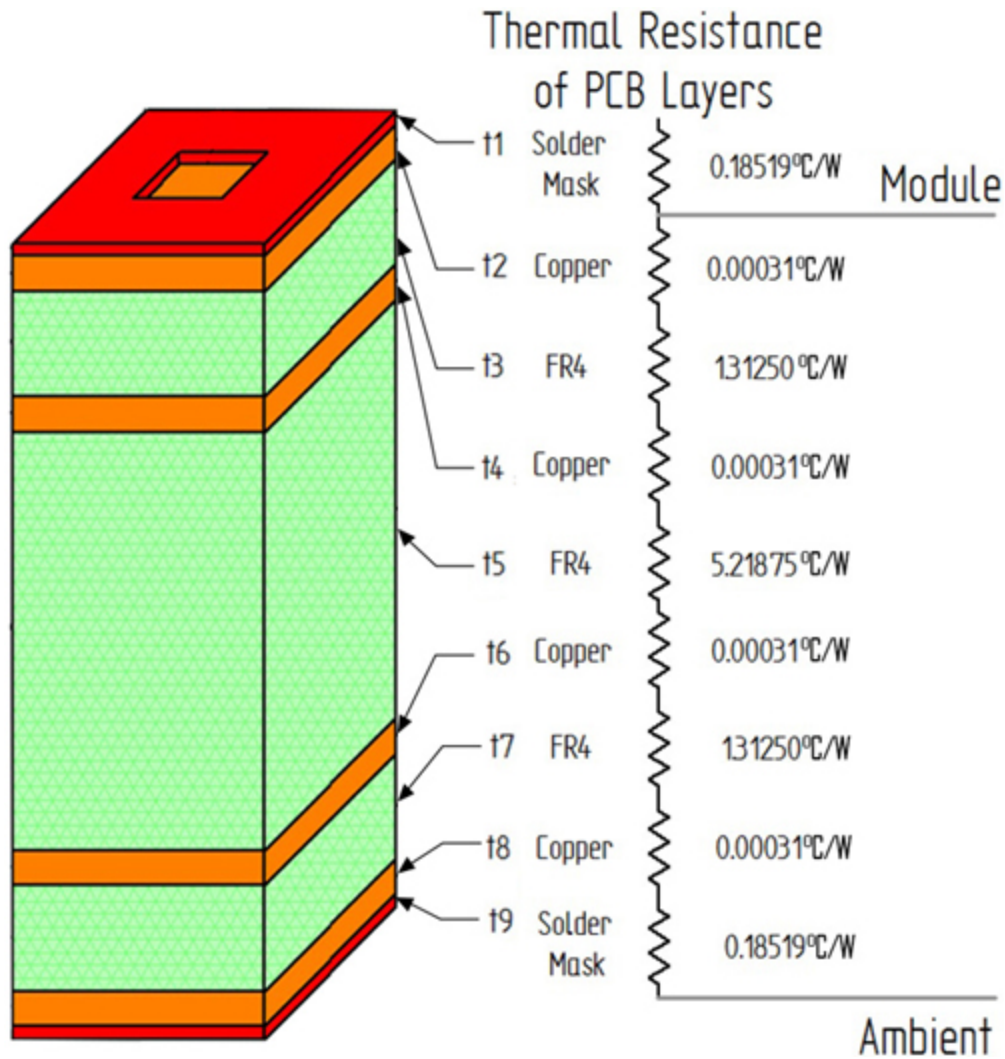


Figure 4. Thermal Resistance of the One Square Inch Board Layers

From these numbers, we can see that the 33.4 mil (t5) layer has the highest thermal impedance. All of the numbers in Figure 4 show the total thermal impedance of one square inch of this four layer board from the top layer to the bottom layer.

What happens if we add one via connection through the board from top to bottom? Let's examine adding that via connection.

Adding Via Connection

The board uses vias that have a finished hole size of about 12 mils (0.012 inches). To build the via, the hole is drilled 0.014 inches in diameter and then plated. The plating adds a copper wall to the inside of the hole that is about 1 mil (0.001 inches) thick. This particular board is also plated using an ENIG process. This adds about 200µin of nickel and about 5µin of gold onto the outer copper surfaces. We will ignore these and just use the copper in our calculations to determine the thermal resistance of the via.

The formula for a cylindrical tube is described in Equation 2.

$$\theta = l/K\pi(r1^2 - r0^2)$$

Equation 2. Cylindrical Tube Calculation

Variable l is the length of the cylinder, K is the thermal conductivity factor, $r1$ is the larger radius and $r0$ is the smaller radius.

Using this equation for the 12 mil (diameter) finished hole we have $r0 = 6$ mils (0.006 inches), $r1 = 7$ mils (0.007 inches) and $K = 9$ for the copper plating.

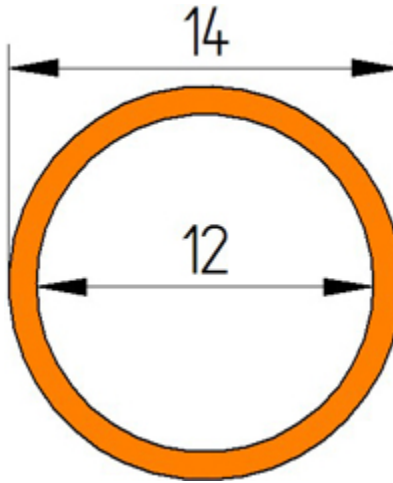


Figure 5. Surface Dimensions of 12 mil Via

Variable l is the length of the via which goes from the top copper layer to the bottom copper layer. There will be no solder mask where the module is soldered to the board, but for other areas, the PCB designer may request that the solder mask be placed on top of each via or the area above the via may be voided. Since the via only connects the outer copper layers, its length is 63.4 mils, or 0.0634 inches. The thermal resistance for the total via length by itself is 167 °C/W as shown in Equation 3.

$$\theta = \frac{0.0614}{9\pi(0.007^2 - 0.006^2)} = 167 \text{ °C/W}$$

Equation 3. Calculation for Thermal Resistance of One Via (12 mils)

In Figure 6, the thermal resistance is listed for each via segment that connects the various layers of the board.

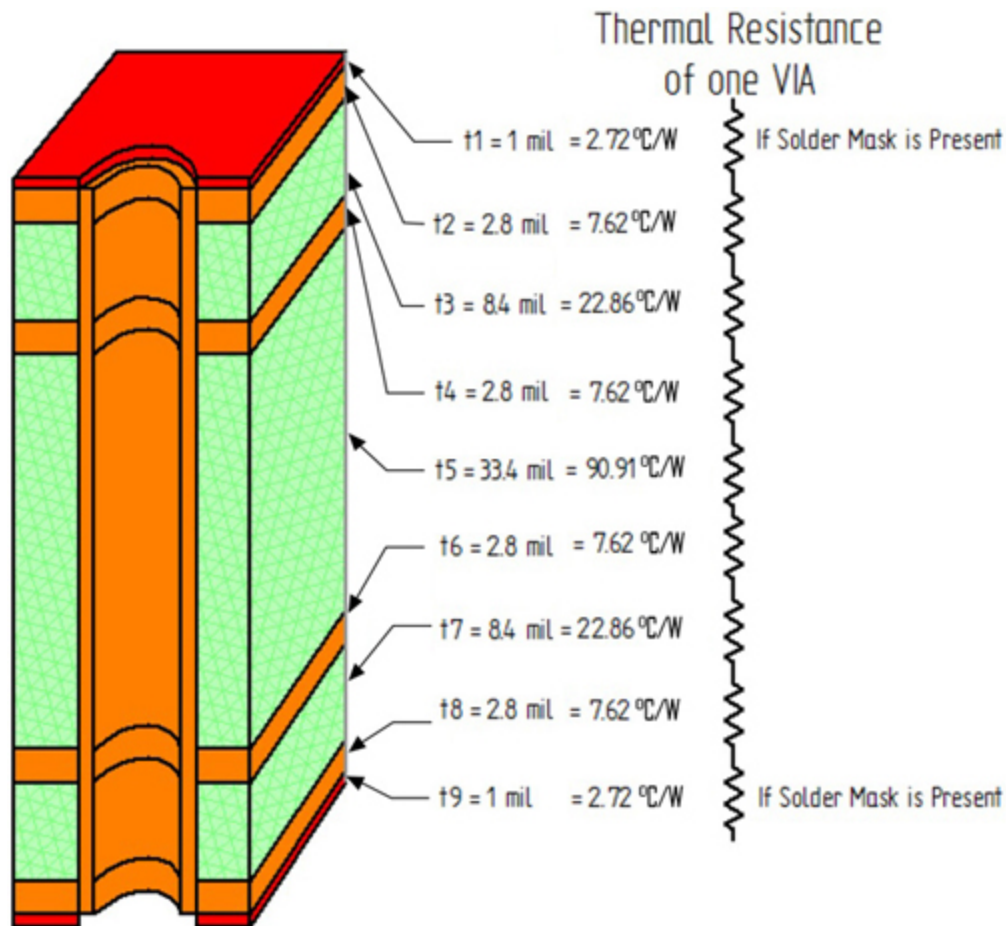


Figure 6. Thermal Resistances for the Via Segments Connecting Each Layer

Note that these values are only the thermal resistance of the one via by itself, not considering that each segment through the board is connected laterally to the materials around it.

If we examine the thermal resistance values of the board layers in Figure 4 and compare them to the thermal resistance values for one via, it appears that the via has much higher thermal impedance for each layer, but note that one via occupies less than 1/5000th of the square inch of board area.

If we decided to compare a smaller board area, say 0.25 inch x 0.25 inch (or 1/16th of the previous board area), the thermal resistance values in Figure 4 would each increase by 16X. For example, the thermal impedance of t4 and the 33.4 mils thick FR4 layer would increase from 5.21875 °C/W to 83.5 °C/W. Adding only one via to this 0.25 inch x 0.25 inch area will reduce the thermal impedance through this 33.4 mils FR4 layer by almost half (83.5 °C/W in parallel with 90.91 °C/W). The area of the 0.25 inch x 0.25 inch square is about 400 times greater than the area of the one via.

So what happens when we place 16 vias in this area? The effective thermal resistance of all the vias in parallel is reduced by 16X when compared to a single via. Figure 7 compares the thermal resistances of the board layers for the 0.25 inch x 0.25 inch segment to that of 16 vias. The 33.4 mil thick FR4 layer of the 0.25 inch x 0.25 inch board has a thermal impedance of 83.5 °C/W. The 16 parallel vias have an equivalent thermal impedance of 5.6821 °C/W.

These 16 vias will occupy less than 1/25th of the area of the 0.25 inch x 0.25 inch board area, but significantly reduce the thermal impedance connections from the top surface to the lower layers.

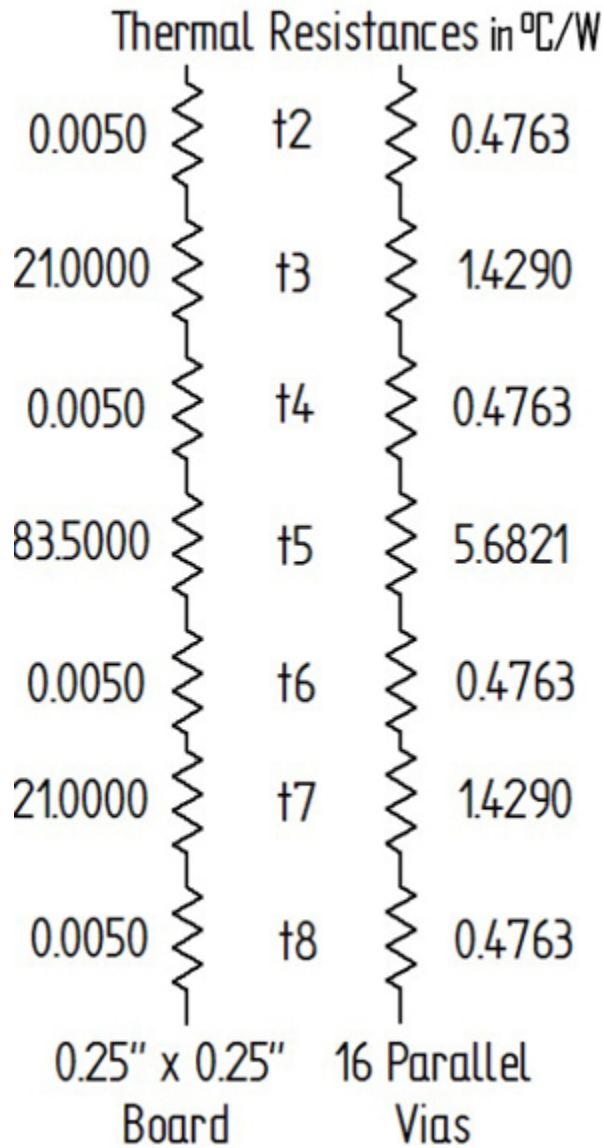


Figure 7. Thermal Resistance Values Comparison

Note that when the heat flows down a via and hits another layer, particularly another copper layer, the heat will move laterally away from the via into that material layer. Adding more and more vias eventually has diminishing returns because the heat moving laterally out of one via into the adjacent material will eventually run into heat coming from another direction that originated from another via.

The ISL8240MEVAL4Z board is 3 inch x 4 inch, and has 2 oz. of copper on the top and bottom layers and two internal layers of 2 oz. copper. To make all this copper useful, the board has 917 12-mil vias, all of which assist in moving heat out of the module, down into the copper layers below.

Conclusion

To address the proliferation of voltage rails and higher performance microprocessors and FPGAs, advanced power management solutions, such as the ISL8240M power module, are offering greater power density and reduced power dissipation for improved efficiency. The optimal implementation of vias in power module board designs has become an increasingly important element to achieving higher power density.

Next Steps

- [Find out more about the ISL8240M power module](#)
- [Get the ISL8240M datasheet](#)
- [Learn more about the ISL8240MEVAL4Z evaluation board](#)
- [Generate a board-level power module design with iSim](#)
- [Learn more about Renesas' power module solutions](#)
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