How to Protect Buck Regulators from Overcurrent Damage

Introduction

Synchronous buck regulators are widely used in industrial and infrastructure applications to step down 12V rails to point-of-load inputs as low as 0.6V for microcontrollers, FPGAs, memory and peripheral I/Os. Overcurrent protection (OCP) is essential to protect these switching regulators from damage by excessive current. Cycle-by-cycle current limiting is typically used due to its fast response. This approach keeps a switching regulator operating continuously with maximum load current, but it can generate excessive heat and potentially reduce system reliability. Second-level protection schemes, such as hiccup-mode and latch-off mode, can be employed to address the reliability concern and improve mean time between failures (MTBF).

This white paper reviews several popular OCP schemes, and explains how these schemes work and how to implement them in buck regulators. We will also discuss the practical considerations examined by power supply designers to help them make the most appropriate choices for their applications.

Overcurrent Protection with Cycle-by-Cycle Current Limiting

The current-mode control (CMC) buck converter has become very popular in recent years because of its many advantages. One of the major advantages is its inherent cycle-by-cycle current limiting by merely clamping the COMP voltage. Figure 1 shows the block diagram of a peak CMC buck converter, which is used as an example to illustrate the various OCP schemes.

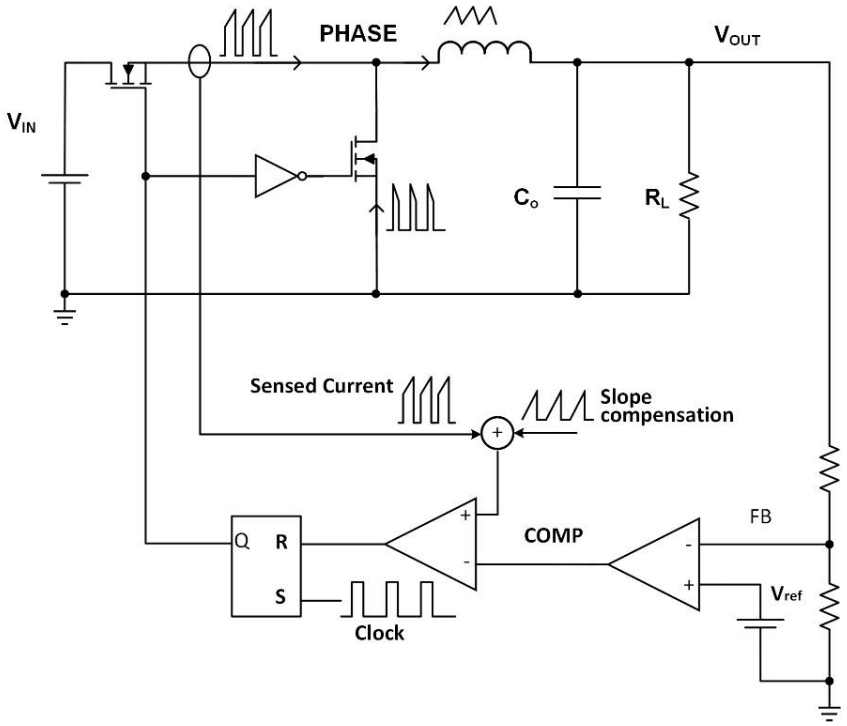

Figure 1. Block diagram of a peak CMC buck converter

The inductor current information needs to be sensed to implement current limiting. The most commonly used current sensing schemes include resistor current sensing, inductor DCR current sensing, power MOSFET RDSon current sensing, and SenseFET current sensing. Due to the high accuracy and negligible power loss, the SenseFET current sensing scheme is widely integrated in switching regulators, such as Intersil's ISL85005 and ISL85014 synchronous buck regulators. SenseFET current sensing is based on the matched devices principle, where the current is split into power FET and senseFET inversely with respect to their resistances. A very high ratio of power FET resistance to SenseFET is often adopted because the current flowing in the SenseFET is only a small fraction of the power FET. Hence, a signal level resistor can be used to sense the current without inserting significant power loss. The first level of OCP with cycle-by-cycle current limiting that power supply designers can implement is A) peak current limiting, followed by B) reverse current limiting. Later we discuss implementing second-level protections for sustained fault events.

A. Peak Current Limiting

In a peak CMC buck converter, the clock signal initiates the switching cycle. Then the high-side switch turns on and the inductor current starts ramping up. The inductor current is sensed and compared to the control signal (V_{COMP}). When the inductor current reaches V_{COMP}, the high-side switch is turned off and the inductor current decreases until the next switching period begins. By clamping V_{COMP}, the peak inductor current can be limited at a desired level. Figure 2 shows the current waveforms operating in normal and current limiting modes.

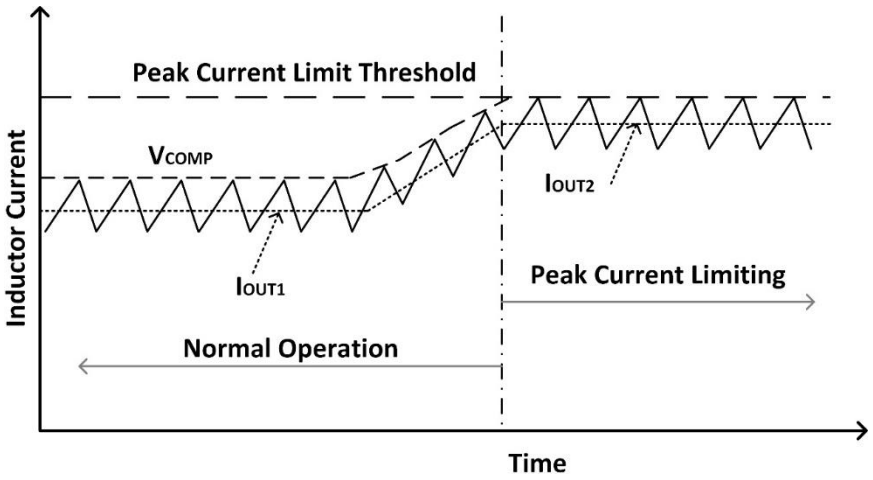

Figure 2. Normal and peak current limiting operation modes

Theoretically, once the inductor current reaches the peak current limiting threshold, the high-side switch on pulse is immediately terminated to keep the inductor current below the peak current limiting threshold. However, a practical PWM controller usually has a minimum on-time limitation. After the clock initiates a new switching cycle, the high-side switch has to stay on for at least a period of minimum on-time before it can be turned off, even if the inductor current reaches the peak current limit threshold.

In a short-circuit fault event, the extremely low output voltage results in slow inductor current decay during the high-side switch off time. The buck converter must operate at a very small duty cycle to keep the inductor current below the peak current limit threshold. In case the on-time demanded by the control loop is less than the minimum on-time, the controller will still keep the high-side switch on for a period of minimum on-time. As a result, the inductor current keeps increasing through each switching cycle, and it eventually exceeds the programmed peak current limit threshold. Two different solutions can be adopted to prevent such a current

runaway due to minimum on-time limitation: Implement a valley current limiting circuit, and/or a switching frequency foldback function as a supplementary protection to peak current limiting.

Valley Current Limiting: Provides an additional level of protection. You can implement valley current limiting by sensing the inductor current when the low-side switch is on. If the sensed current at the end of the switching cycle exceeds the valley current limiting threshold, the high-side switch will skip the next cycle and remain off until the current decays below the valley current limiting threshold. Thus, the previously discussed current runaway situation (due to minimum on-time) can be avoided. Figure 3 shows an example illustrating this protection mechanism.

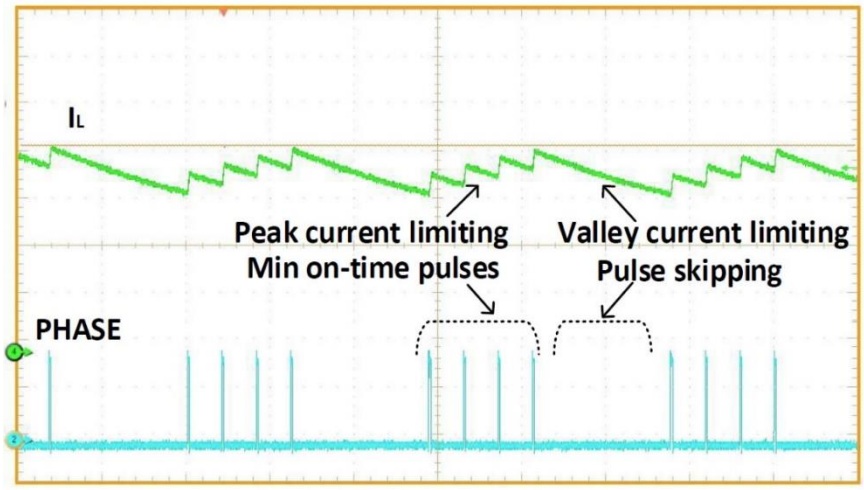

Figure 3. Peak current limiting along with valley current limiting

Switching Frequency Foldback: Provides another effective approach to eliminate current runaway risk caused by minimum on-time in a short-circuit fault event. When an overcurrent event is detected, the peak current limiting circuit limits the duty cycle and thus decreases the output voltage. When the feedback voltage and/or on-time is lower than the programed threshold, the frequency foldback function reduces the switching frequency. Having lower frequency for a demanding duty cycle will produce a longer on-time. Keeping the frequency low enough (so the demanding on-time is larger than the minimum on-time) will avoid the current runaway situation. The reduced frequency also results in larger inductor current ripple and lower output current. The frequency will automatically recover to the normal value after the short-circuit fault is removed.

B. Reverse Current Limiting

In a non-synchronous buck converter with diode rectification, inductor current is always positive. In contrast, inductor current in a synchronous buck converter can flow in either direction through the low-side MOSFET when it operates in forced continuous conduction mode (FCCM). In case output voltage is accidently lifted above the output setting point, a large negative current will flow from V_{OUT} to the PHASE node and through the low-side MOSFET to ground. Excessive reverse current can also lead to regulator failure.

As we've discussed, both peak current limiting and valley current limiting can only limit the forward current, but not the reverse current. An additional reverse current limit circuit is required. It will force the low-side MOSFET off in response to the reverse current flowing through it, thereby exceeding a preset reverse current limiting threshold.

Second-level OCP Schemes

Cycle-by-cycle current limiting provides prompt first level protection by limiting the maximum current at a preset level. A switching regulator operating with continuous maximum current suffers from high temperature rise, and may even reach the thermal shutdown threshold in some scenarios. When that happens, a thermal shutdown protection circuit will shut off the switching regulator to prevent damage. When the regulator turns off, it will start to cool down. Once the regulator has sufficiently cooled off, it will automatically recover from thermal shutdown. In a sustained fault event, the regulator cycles between peak current limiting and thermal shutdown, causing harm to the regulator's long-term reliability. Two second-level protection mechanisms (hiccup mode or latch-off mode) should be considered to address this concern and improve MTBF.

Hiccup Mode Protection: This protection is usually implemented with cycle-by-cycle peak current limiting along with a cycle count circuit. Hiccup operation is initiated when an overcurrent event is detected. The cycle-by-cycle limiting circuit acts to limit the peak current. Then the cycle count circuit counts the switching cycles. After a certain number of consecutive cycles, the switching regulator is turned off for a given time, and then attempts to start up again. If the overcurrent condition has been removed, the switching regulator will start up and return to normal operation. Otherwise, it will see another overcurrent event and shut off again, repeating the previous cycle.

In a sustained fault condition, the regulator only operates for a short duration in the hiccup cycle, as shown in Figure 4. During hiccup mode, power dissipation and temperature is much lower. As a result, power supply reliability is improved versus regulators with only cycle-by-cycle current limiting.

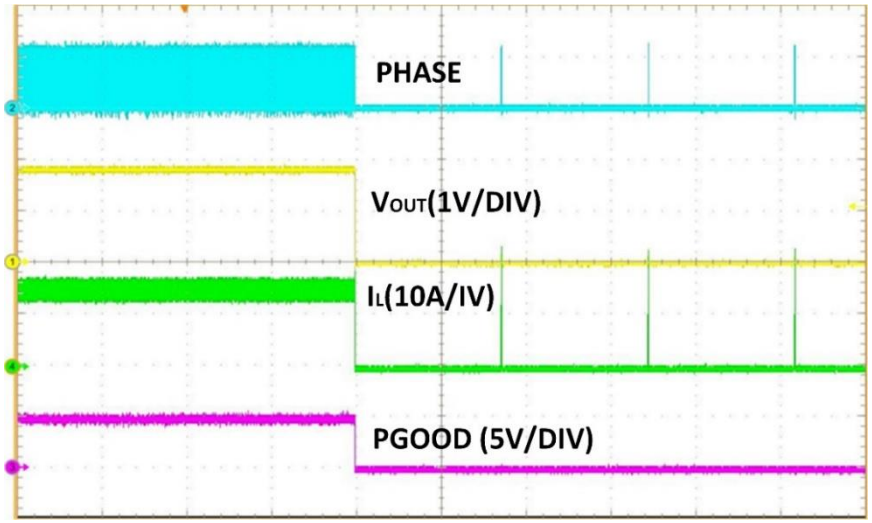

Figure 4. Hiccup mode OCP in a sustained fault condition

Latch-off Mode Protection: Like cycle-by-cycle current limiting schemes, hiccup mode OCP also enables the regulator to restart after the fault is removed. While the auto-recovery feature is popular in many applications, latch-off mode protection might be preferred in some other applications, such as battery power systems to eliminate unnecessary battery drain in sustained fault conditions. As shown in Figure 5, the latch-off mode protection shuts down the regulator and latches it off when an overcurrent event is detected. Toggling off ENABLE or V_{IN} will be required in order to restart the regulator.

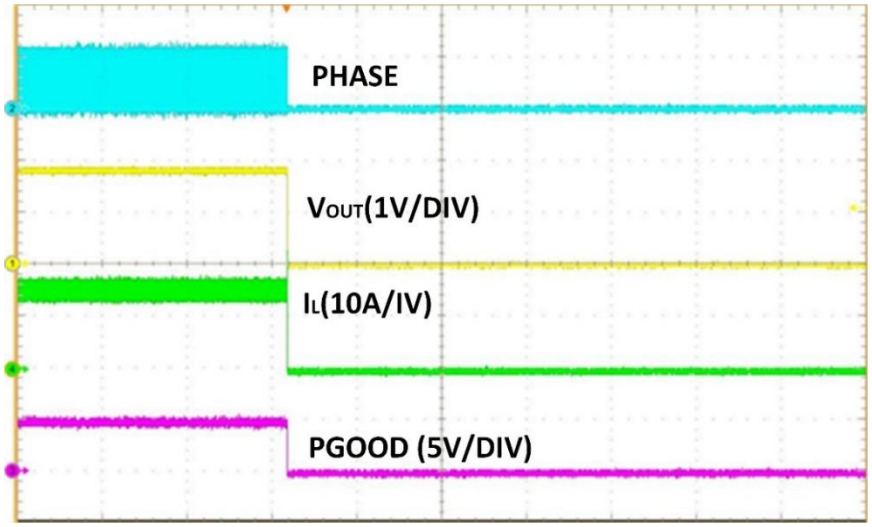

Figure 5. Latch-off mode OCP

Many advanced integrated switching regulators have built-in OCP circuits to protect themselves from excessive current and power dissipation. Different switching regulators might provide various protection schemes. The ISL85003, ISL85005, and ISL85005A synchronous buck regulators from Intersil have internal peak current limiting, valley current limiting and reverse current limiting functions to provide comprehensive protections. The ISL85009, ISL85012, and ISL85014 synchronous switching regulators also have these current limiting functions. In addition, they offer a frequency foldback function, and hiccup mode and latch-off mode protection options to fully protect the switching regulators and enhance system reliability.

Conclusion

Power supply designers should make appropriate choices based on their practical applications requirements. Cycle-by-cycle peak current limiting provides switching regulators fast protection from excessive current by limiting the inductor peak current. To overcome the failure of peak current limiting, due to minimum on-time limitations, consider employing additional valley current limiting and/or frequency foldback. And remember, reverse current limiting protects against large negative sink current. As a second level protection, hiccup mode protection enhances the system reliability by reducing power dissipation and lowering temperature rise. In case the auto-recovery feature is not desired in sustained fault conditions, latch-off mode protection should be selected.

Next Steps

- Learn more about the ISL850xx regulators
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